EXPERIMENT X. BASIC AND STANDARD TTL INVERTERS

I. Introduction

I.1 Objectives
In this experiment, you will analyze and compare the voltage transfer characteristics (VTC) and the dynamic response of the basic and standard TTL inverter. You will use Visual Engineering Environment (VEE) for controlling the laboratory instruments

- DC power supply (Agilent E3631A) and
- Digital multimeter (Agilent 34401A)

for sending and receiving data. You will manipulate this data to display the VTC of TTL inverters.

II. Preliminary Work

1) Read Chapter 7 (Transistor-Transistor Logic [TTL]) of Digital Integrated Circuits by T. A. Demassa and Z. Ciccone.

2) Read your EE312 course notes for information on TTL inverters.
3) Consider the basic TTL inverter given in Fig. 1. Assume that $V_{BE}(FA)=0.7 \, \text{V}$, $V_{BE}(SAT)=0.8 \, \text{V}$, $V_{CE}(SAT)=0.2 \, \text{V}$, $V_{BC}(RA)=0.7 \, \text{V}$, $\beta_F=50$, $\beta_R=0.1$. Use $\sigma_0=0.8$ (saturation parameter of $Q_0$) for the output low state.

i) Find the operation mode of each BJT and $I_{IN}$, $I_{RB}$, $I_{RC}$, $I_{B2}$ when $V_{in}=0 \, \text{V}$ and $V_{in}=5 \, \text{V}$.

ii) Sketch the **voltage transfer characteristics** by finding $V_{OL}$, $V_{OH}$, $V_{IL}$, $V_{IH}$.

iii) Find the **noise margins**.

iv) Find the **maximum fanout**. What is the limiting case for determining the fan-out limit of this circuit?

![Fig. 1: The schematic view of a basic TTL inverter](image)

4) What are the **advantages** of the basic TTL inverter when compared with the basic BJT inverter (RTL inverter that you also constructed in Experiment 2)? What are the limitations of the circuit?
5) Consider the standard TTL inverter given in Fig. 2. Assume that $V_{BE}(FA)=0.7$ V, $V_{BE}(SAT)=0.8$ V, $V_{CE}(SAT)=0.2$ V, $V_{BC}(RA)=0.7$ V, $\beta_F=50$, $\beta_R=0.1$, $V_{DIODE(ON)}=0.7$ V. Use $\sigma_O=0.8$ (saturation parameter of $Q_0$) for the output low state.

i) Sketch the **voltage transfer characteristics** by finding $V_{OL}$, $V_{OH}$, $V_{IL}$, $V_{IH}$, $V_{IB}$, $V_{OB}$.

ii) Find the **noise margins**.

iii) Find the **maximum fanout**. What is the limiting case for determining the fan-out limit of this circuit?

iv) Find the **average power dissipation** when there is no load.

---

**Fig. 2: The schematic view of a standard TTL inverter**

6) What are the **advantages** of the standard TTL inverter when compared with the basic TTL inverter?

7) Read the **Displaying Voltage Transfer Characteristics with VEE** section in **Experiment 2**. Bring the **Experiment 2 manual** with you when you come to the laboratory.
III. Experimental Work

a) Basic TTL Inverter

Fig. 3 and Fig. 4 show the schematic view of a TTL inverter circuit and the internal diagram of **CA3046 BJT** array chip. Construct the TTL inverter circuit by using **two npn BJTs** in CA3046. Connect pin 13 to ground.

![Schematic View of a Basic TTL Inverter](image1)

**Fig. 3: The schematic view of a basic TTL inverter**

![Pin Diagram for CA3046 BJT Array Chip](image2)

**Fig. 4: Pin diagram for CA3046 BJT array chip**
1) Use the **multimeter** in **voltage measuring mode** to find the operation modes of the BJTs for $V_{IN}=0V$ and $V_{IN}=5V$.

2) Obtain the **voltage transfer characteristics** of the basic TTL inverter with the help of VEE. Set $V_{CC}=5V$. **Sweep** the $V_{IN}$ from 0 V to 5 V in 0.05 V steps.

3) Find the critical voltages, $V_{IL}$, $V_{IH}$, $V_{OL}$, $V_{OH}$ and **noise margins**. Why the difference between $V_{IL}$ and $V_{IH}$ is small? Why is the low noise margin much smaller than the high noise margin?

4) Measure the emitter current of Q1 for $V_{IN}=0$ and $V_{IN}=5V$.

5) Explain the operation of this inverter.

6) What is the limiting case for determining the fan-out limit of this circuit? Comment briefly on what is expected when $V_{OUT}=V_{OH}$.

7) Find the fan-out limit of the circuit for $V_{OUT}=V_{OL}$. Connect the **circuit input** to $V_{CC}$ and connect a **potentiometer between** the **output** and $V_{CC}$. Change the potentiometer resistance and record the current through the resistor when $V_{OUT}$ exceeds the acceptable low level voltage.

8) Ground the circuit input and connect a resistance between the output and ground with a value equivalent to the **fan-out of 1**. Measure the output voltage and comment on the result. What is the limitation of this circuit? How can the circuit be improved for a reasonable fan out limit?

9) In this part, we will measure the rise and fall times of the basic TTL inverter with VEE. Disconnect the input of the circuit from the power supply. Connect a **100 pF capacitor** between the output and ground. Set the output of the function generator to **High Z**. Connect the input of the circuit to the output of the function generator and set the waveform to a square wave with 5 $V_{PP}$ amplitude and 2.5 $V$ offset at a frequency of 1 kHz. Connect the **channel 1** of the oscilloscope to the **output**.

Since there are two types of oscilloscope in the laboratory and their drivers are not the same, we will use different VEE configurations for them.
i) Configuration for 54645D Oscilloscope Using Plug & Play Drivers

- From Instrument Manager, click on HP54645D and then PNP button and place the Plug & Play Driver in the work area.

- Double click on the <Double-Click to Add Operation> bar of the driver. Select WaveformArray_Q under Waveform. From the Panel tab, select Analog Channel 1.

- Add an X vs Y Plot object. Connect W_Time and W_Volt data output pins of the Plug & Play Driver to the XData and YData1 pins, respectively.
ii) Configuration for MSO-X2012A Oscilloscope Using IVI Drivers

- From Instrument Manager, click on MSOX2012A and then IVI button and place the IVI Driver in the work area.

- Double click on the <Double-Click to Add Operation> bar of the driver. Select CreateInstance and click OK. Click OK in the opened Edit "CreateInstance" window.

- Double click on the <Double-Click to Add Operation> bar of the driver. Select Initialize and click OK. Enter simulate=false into the OptionString field and click OK.

- Double click on the <Double-Click to Add Operation> bar of the driver. Select Channels → Item(Name) → FetchWaveform and enter channel1 into the Name field.

- The input pins of the driver should be connected. Hence, add a Real64 constant and a Real64 Array constant in the work area. Connect the data output pin of Real64 Array to the WaveformArray input pin of the driver. Connect data output pin of Real64 to the InitialX and Xincrement input pins of the driver. The values of Real64 constant objects are not important.

- Place an AllocReal64 object in the work area. Add two data input pins which are From and Through. Enter 50000 as the size.

- Add a Formula object. Add an additional data input, B. Enter A+49999*B into the formula box. Connect the InitialX data output pin of the driver to A pin of Formula. Connect the Xincrement data output pin of the driver to B pin of Formula.

- Connect the Return data output pin of Formula to Through pin of the AllocReal64 object. Connect the InitialX data output pin of the driver to From pin of the AllocReal64 object.

- Add an X vs Y Plot object. Connect Array pin of AllocReal64 to the XData pin. Connect the WaveformArray output pin of the IVI driver to the YData1 pin.
10) Run the VEE program and measure the rise and fall times of the output.

11) You can interpolate the data if necessary. For this purpose, click on X vs Y Plot object. From the Properties box, change MarkerInterpolate value to True under Markers.
b) 74LS00 TTL NAND Gates

Fig. 5 shows the pin diagram of 74LS00 and the internal structure of one of the NAND gates. Insert 74LS00 IC into your breadboard. Connect pin 14 to 5 V and pin 7 to ground. Connect a 10 nF capacitor between \( V_{CC} \) and ground.

![Pin Diagram of 74LS00 and Internal Structure](image)

**Fig. 5:** The pin diagram of 74LS00 and the internal structure of one of the NAND gates

1) Leave the other pins unconnected and measure the voltages on pins 1, 2, 3, 4, 5, 6, 8, 9, 10, 11, 12, and 13. Comment on the results.

2) Now use one of the NAND gates in the IC. **Short circuit the two inputs** and obtain the **voltage transfer characteristics** with the help of \( V_{EE} \). Set \( V_{CC} = 5 \) V. **Sweep** the \( V_{IN} \) from 0 V to 5 V in 0.05 V steps.

3) Find the critical voltages, \( V_{IL}, V_{IH}, V_{OL}, V_{OH} \) and **noise margins**.

4) Measure the input currents under high and low level input conditions.

5) Connect the inputs to ground. Connect a resistor equivalent to a **fan-out of 15** between the output and ground and measure the output voltage. Compare the fanout limitation of this circuit (schematics shown above) with the circuit in Part 1 of Experimental Work (TTL inverter). Comment on the result by stating the reason for higher fan-out in this circuit.
6) Disconnect the resistor connected at the output. Connect a **100 pF capacitor** between the output and ground. Apply a **5 V<sub>pp</sub> square wave** of **1 kHz** frequency and **2.5 V offset** at the input and measure the **rise** and **fall times** of the NAND gate using VEE and compare them with those measured in **Part a** of Experimental Work. State the reasons of any differences you observe in the switching times of this circuit and the circuit in **Part a**.