MIDDLE EAST TECHNICAL UNIVERSITY

DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING

EE 314 - DIGITAL ELECTRONICS LABORATORY **SPRING 2014-2015**

PRACTICAL FINAL

May 11-15, 2015 (000)
90 min

INSTRUCTIONS

- Read all of the instructions and all of the questions before beginning the exam.
- There are 3 questions on this exam, totaling 18 points.
- Do not spend all your time on one problem and on one part and attempt to solve all of them.
- You must show your work for all problems to receive full credit; simply providing answers will result in only partial credit, even if the answers are correct.
- Turn in the entire exam, including this cover sheet.
- Put your name on any additional material that you submit.
- Be sure to provide units where necessary.
- Please indicate the number of page where your work is to be continued.

Last Name :……

Name :……

Section :……

Student No :……

Q		Grade
1	6	
2	6	
3	6	
Total	18	

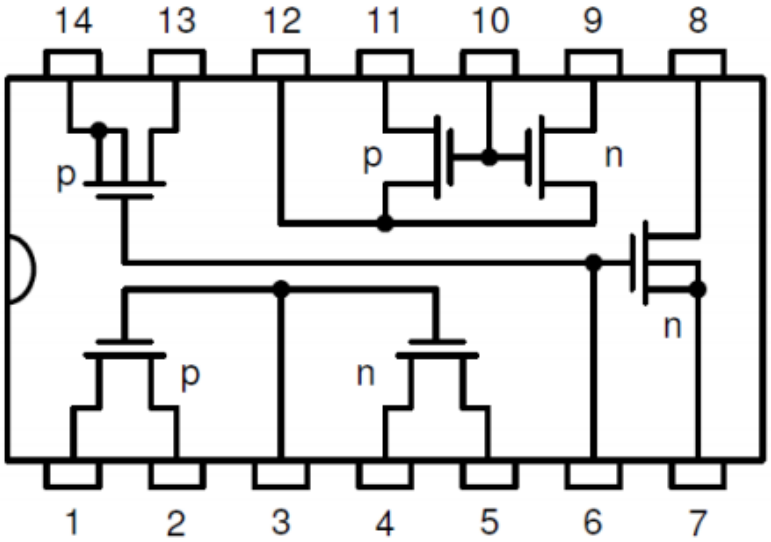
PART A

1) Design a **3-input CMOS logic gate** which realizes the function **Y=(A(B+C))'** (**complement of A(B+C)**).

Draw your design here:

2) Construct the gate you designed on breadboard using **NMOS** and **PMOS** transistors in **CD4007 MOS array chip** whose pin diagram is given below. Do not forget to connect **pin 7** to **ground** and **pin 14** to $\mathbf{V_{DD}}$.

Be careful with using CD4007 MOS chip. Some NMOS and PMOS transistors are connected to each other internally. Use more than one CD4007 if needed.



3) Connect the **B and C inputs** of the gate to **ground**. Obtain the **voltage transfer characteristics** of your design using **VEE**. For this purpose, you will use **DC power supply** to sweep the **input voltage** and **multimeter** to read the **output voltage**. You are required to use **IVI drivers** for both. You will sweep $\mathbf{V_{IN}}$ from **0** to **5 V** in **0.2 V steps** for $\mathbf{V_{DD}}$**=4 V and 5 V**.

Hints:

- For the IVI driver of DC Supply, **output1** and **output2** are the names for **6 V** and **25 V** outputs, respectively.
- You can select **current limit** as **100 mA** for DC supply outputs.
- While initializing IVI drivers, please use the following settings:

	HPE3631A IVI Driver (DC Power Supply)	**HP34401A IVI Driver (Multimeter)**
IdQuery	**True**	**True**
Reset	**False**	**True**
OptionString		**simulate=false**

4) After obtaining desired voltage transfer characteristics, **call your assistant** to show your **breadboard, design in VEE and plot**.

PART B

The following question will be answered using **Quartus II.**

- Create a new project on "Desktop".
- Build the hierarchical component in Figure 1 and create a new symbol using the schematic. Note that DEC38 is a 3x8 decoder. You can find it within the component list.

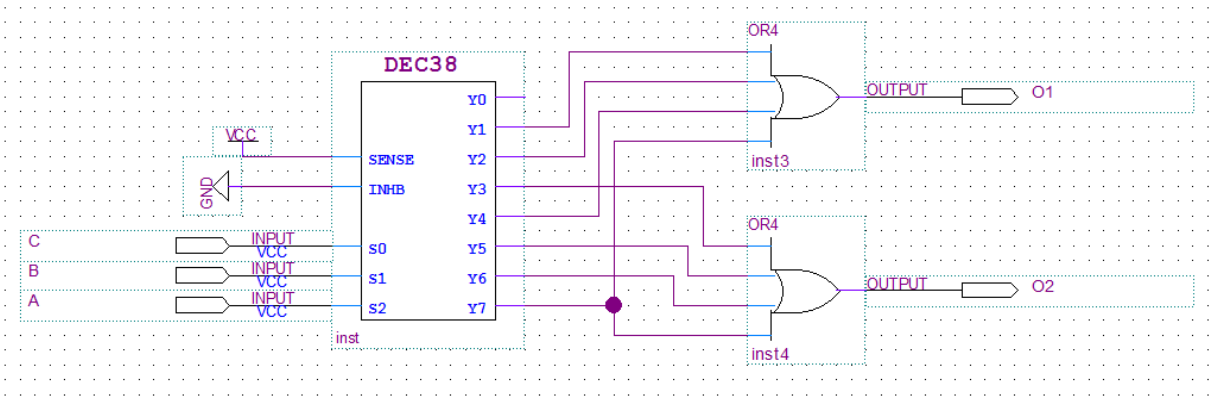


Figure 1 (Block named as 'first' in Figure 2)

- What is the function (name) of this component (Figure 1)?

_____

- Using the symbol block you have just buit, draw the circuit given in Figure 2 as the top-level schematic file.

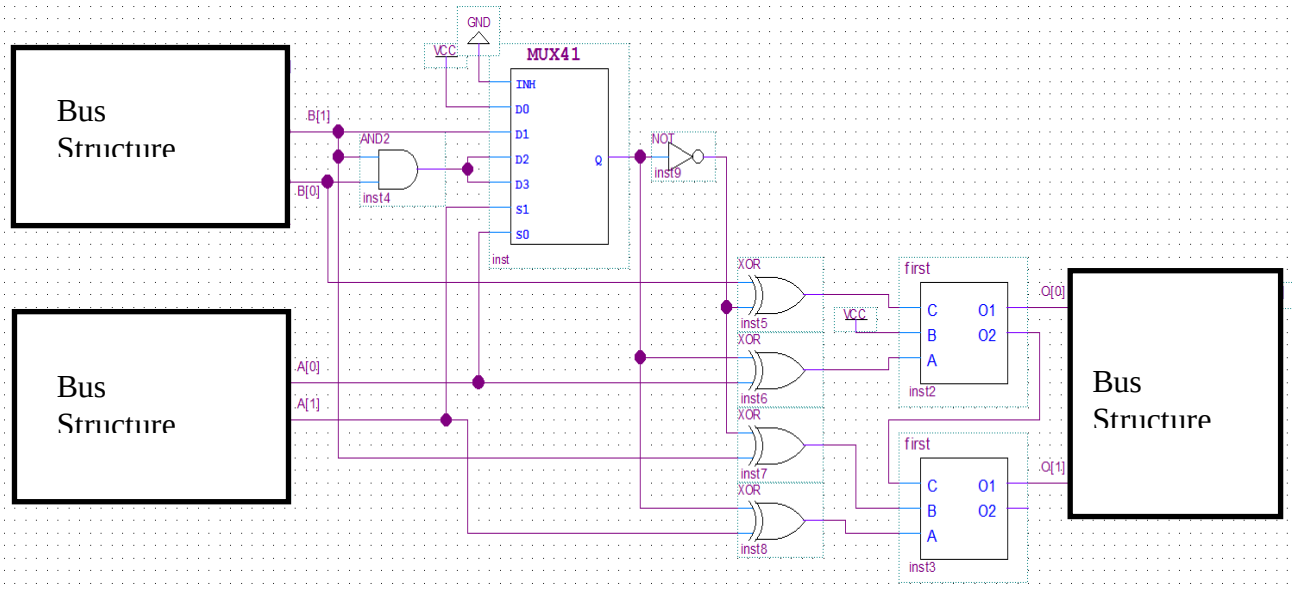


Figure 2

- What is the function (name) of this component (Figure 2)?

_____

- Simulate the circuit in Figure 2 such that following inputs are applied consecutively and fill in the table below. **Make sure** to use bus structure for inputs.

A (A_1A_0)	**B (B_1B_0)**	**A (O_1O_0)**
1 (01)	3 (11)	
3 (11)	2 (10)	
0 (00)	0 (00)	
1 (01)	2 (10)	
2 (10)	3 (11)	
0 (00)	2 (10)	
3 (11)	0 (00)	

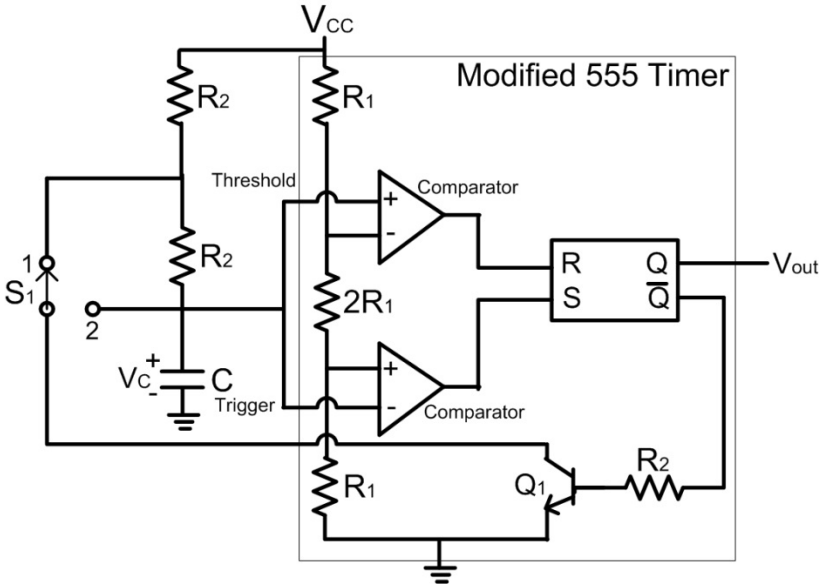
- Now implement the circuit on FPGA and **display both simulation and implementation results to your assistant.** Make sure that the operations listed above are displayed consecutively in the simulation window with **bus structures** organized as **binary**.

  Just raise your hand and wait for your assistant to come and check your monitor. Make sure that the display is ready. You have just one chance to have your results checked, assistants will not visit any desk a second time.

- When your assistant has checked your simulation and implementation, he/she will also check the schematics.
- After the assistant has left your PC, close any schematic editor and simulation windows.
- Close Quartus II.
- Delete your project.

PART C

Consider the circuit implementation using a modified 555 Timer. Assume that the transistor Q_1 is always in saturation as long as Q = 0.



BJT
β = 20
$\mathbf{V_{CE,SAT}}$ = 0 V
$\mathbf{V_{BE,SAT}}$ = 0.8 V
$\mathbf{V_{D(ON)}}$ = 0 V

$\mathbf{V_{CC}}$ = 8 V
$\mathbf{R_1}$ = 2 kΩ
$\mathbf{R_2}$ = 200 Ω
C = 0.1 µF

Indicating all critical voltages, determine and plot $v_c(t)$ and $v_{out}(t)$ from t = 0 up to t = $3R_2C$ assuming

1) the capacitor is initially charged to V_{CC}.
2) the switch S_1 is initially connected to position "1".
3) the switch S_1 changes position as a function of time as given below: