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GENERAL RULES FOR EE314 PROJECTS

Followings are the important points about projects:

- This year we are offering 5 projects. Please note that during weekends, laboratory will be closed. In order to work efficiently, try to complete your project in simulation domain as much as possible and try not to spend too much time for debugging.

- The aim of the projects is to make you more familiar with some subjects you were introduced in digital electronics and logic design. However, you may need to do some research and study extra material to accomplish the task. This will be a good first step for 4th year graduation projects.

- The design approach that you will use is not limited. You are free and encouraged to use your own ideas to improve the projects. Therefore, sky is the limit!

- The project groups will contain 2 students.

- It is not necessary that your lab partner and project partner is the same person.

Projects: #1-Peace by Fatih Çakır and Emre Alp Miran, #2-War by Fırat Öcal and Fatih Mehmet Özçelik, #3-Dipole by Yunus Can Gültekin and Mustafa Kangül, #4-Hürkuş (Freebird) by Kübra Çırçır and Özlem Tuğfe Demir, #5-Road Runner by Eren Aydın and Mahmut Kamil Aslan. Project coordination by Mustafa Kangül, and Barış Bayram (e-mail: mustaf.kangul@gmail.com)

- There are responsible assistants for each project. It is recommended that you ask your questions via e-mail to those assistants.

- There will be no mid-report.

- Project demonstrations will be held on the first week of the June.

- Early demonstration possibility should be discussed with your project assistant.

- Final reports will be submitted during demonstrations.

- Soft copy of final report will be submitted.

- Example report can be found on ODTUCLASS system.

How to get a ZERO grade from project:

- Copying code fragments or modules directly from an internet source,
- Sharing modules and code parts between project groups,
- Fully copying another group's code and other project work,
- Any other action that puts you at an unjust advantage over other project groups.

In the projects you will use Altera DE1-SoC board. In the demonstrations computer monitors will be used for screen display. In order to drive monitors you have to use VGA port of the board. Following information will be helpful for VGA interface.

VGA interface:

VGA is a widely used standard in video industry for the transmission of video signals from a computer or microprocessor into a monitor or TV. Each 640x480 image is called a 'frame' and each frame contains 480 lines which are made up of 640 pixels.

The monitor starts displaying each frame by beginning from the first line and then the first pixel of this line. In each line, the display order is from left to right; and each frame is written in an order from top to bottom. So, your first pixel is always at the top left corner, while the last pixel at the bottom right.

You will need to generate an image buffer with at least 640x480 = 307200 bits to store each line and frame in order to form a coherent image; however you will also need to adjust two synchronization signals called HSync (Horizontal Synchronization) and VSync (Vertical Synchronization) in order to see a video. These signals tell the monitor when a line or frame is finished, and the monitor should start from the next line or frame.

As shown in Figure 3, VGA interface is actually very simple, and you will only need to make 3 connections, namely R-G-B. For example, for a white pixel all three inputs should be high, and for a black pixel the inputs should be low. The FPGA cards in the laboratory already have a VGA output port with color outputs, so you will only need to supply the R-G-B data digitally to the VGA port. Necessary pins for these assignments can be found in the user manual. (http://www.terasic.com.tw/cgi-bin/page/archive_download.pl?Language=English&No=836&FID=eac30a7aaacf5187a4ace0d613cd4676)

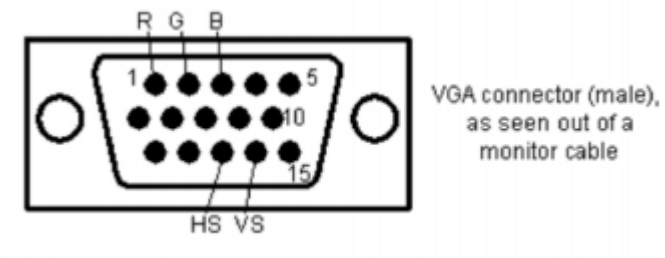

Figure 1: VGA interface.

HSync and VSync: HSync and VSync are necessary in order to tell the monitor to ‘start’ or ‘stop’ writing a line or frame. You will need to build the necessary digital blocks in order to correctly form these two signals. These blocks are basically counters with some modifications and are very easy to implement in Verilog. You can see the horizontal and vertical synchronization signals in Figure 2 with the corresponding timing in Table 1.

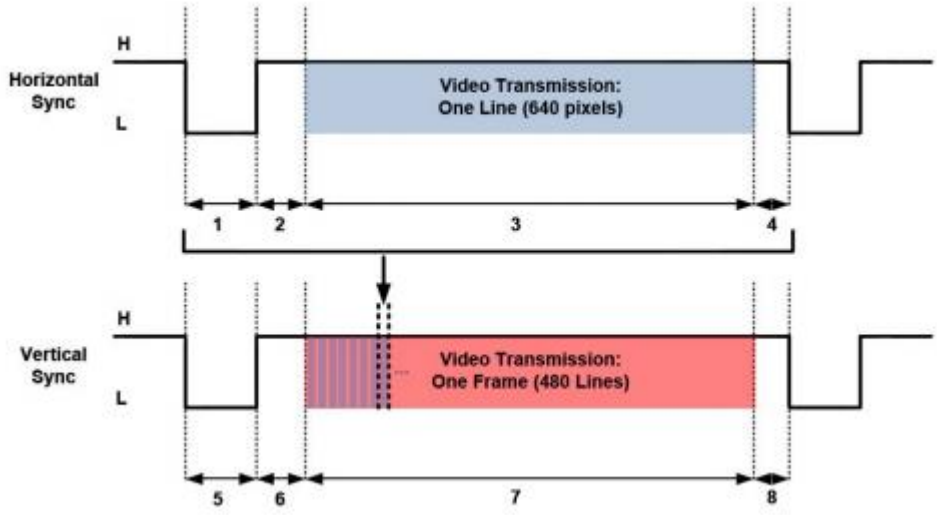

Figure 2: HS and VS.

Timeline # on Fig. 1	Name	Duration	Clock Count
1	H. Sync	3.84 µs	96
2	Back Porch (H)	1.92 µs	48
3	Video Signal (One Line)	25.6 µs	640
4	Front Porch (H)	0.64 µs	16
5	V. Sync	0.064 ms	2
6	Back Porch (V)	1.056 ms	33
7	Video Signal (One Frame)	15.36 ms	480
8	Front Porch (V)	0.32 ms	10

Table 1: Timing.

By observing Figure 2 and Table 1, we can understand that the HSync signal is used to synchronize one line in a frame, while VSync is used to synchronize each frame. Basically, when HSync or VSync is low, the monitor understands that it needs to switch from one line or frame to the next. Back and front porch are idle stages where the monitor is getting ready to write the next pixel or line. They also include 8 pixel and line over scan or 'border' pixel/lines outside our standard view of the monitor.

IMPORTANT NOTE: The video input signals (R, G, B) of a VGA monitor should be off (or black) during H. or V. Sync stages, and front/back porch stages. The video input signals should only be active during an active video transmission stage, which are highlighted in Figure 2.
In order to construct these HSync and VSync signals and to achieve transmission of each line/pixel, you will need a 25 MHz clock signal. This

will also mean that each pixel will be transmitted at 25 MHz to the monitor during active video stages.
Internal clock information about ALTERA can be found under the Clock Circuitry part of the user manual.

http://www.epanorama.net/documents/pc/vga_timing.html
http://martin.hinner.info/vga/640x480_60.html