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# **EXPERIMENT 6.** CMOS INVERTERS AND CMOS LOGIC CIRCUITS

# I. Introduction

#### I.I Objectives

In this experiment, you will analyze the voltage transfer characteristics (VTC) and the dynamic response of the CMOS inverter and gain experience in some CMOS logic circuits. You will use Visual Engineering Environment (VEE) for controlling the laboratory instruments

- DC power supply (Agilent E3631A) and
- Digital multimeter (Agilent 34401A)
- Function generator (Agilent 33120A, 33220A) for sending and receiving data.

# II. Preliminary Work

- **1)** Read section **4.10** (The CMOS Digital Logic Inverter) of Microelectronic Circuits by Sedra/Smith (5<sup>th</sup> edition).
- 2) Read sections 10.1-10.3 (in Digital CMOS Logic Circuits) of Microelectronic Circuits by Sedra/Smith (5<sup>th</sup> edition).
- **3)** Read sections **23.1-23.5** (in **CMOS Inverter**) of **Digital Integrated Circuits** by **T. A. DeMassa** and **Z. Ciccone**.

**4)** Consider the CMOS inverter given in Fig. 1. What are the states of Q<sub>N</sub> and Q<sub>P</sub> for the critical points **V**<sub>IL</sub>, **V**<sub>IH</sub>, **V**<sub>OL</sub>, **V**<sub>OH</sub>, and **V**<sub>M</sub> ?



Fig. 1: The schematic view of a CMOS inverter

#### 5)

- i) For the CMOS inverter given in Fig. 1, determine the critical voltages  $V_{IL}$ ,  $V_{IH}$ ,  $V_{OL}$ ,  $V_{OH}$ , and  $V_{M}$ . Let  $V_{DD}$ = 5 V,  $V_{T,N}$ =- $V_{T,P}$ =1.5 V,  $(W/L)_N$ = $(W/L)_P$ =5,  $k_N'$ = $k_P'$ =20  $\mu$ A/V<sup>2</sup>. Find the noise margins.
- ii) Repeat part i) for  $V_{DD}$ = 5 V,  $V_{T,N}$ =- $V_{T,P}$ =1.5 V,  $(W/L)_N$ =5,  $(W/L)_P$ =5,  $k_N'=k_P'=100 \ \mu A/V^2$ .
- iii) Repeat part i) for  $V_{DD}$ = 5 V,  $V_{T,N}$ =- $V_{T,P}$ =1.5 V,  $(W/L)_N$ =5,  $(W/L)_P$ =15,  $k_N'=k_P'=20 \ \mu A/V^2$ .
- iv) Repeat part i) for  $V_{DD}$ = 5 V,  $V_{T,N}$ =- $V_{T,P}$ =1.5 V,  $(W/L)_N$ =15,  $(W/L)_P$ =5,  $k_N'=k_P'=20 \ \mu A/V^2$ .
- **v**) Comment on the effect of  $\mathbf{k}_N = \mathbf{k}_N'(\mathbf{W}/\mathbf{L})_N$  and  $\mathbf{k}_P = \mathbf{k}_P'(\mathbf{W}/\mathbf{L})_P$  on the critical voltages and noise margins using the results of the previous parts.

- 6) Design a 3-input CMOS NAND gate and draw it. Specify (W/L) ratios for all transistors in terms of the ratios  $n=(W/L)_N$  and  $p=(W/L)_P$  of the basic inverter, such that the worst case gate delay is equal to that of the basic inverter.
- 7) Design and draw a CMOS logic circuit that realizes the function Y=A'+B'D'+C'D' using 8 transistors. Specify (W/L) ratios for all transistors in terms of the ratios n and p of the basic inverter, such that the worst case gate delay is equal to that of basic inverter. Note that complements of the signals are available.
- 8) Consider the NMOS pull-down section of a CMOS gate in Fig. 2. Draw the pull-up section of this gate. Write the expression of the logic function performed by this CMOS gate. Provide transistor (W/L) ratios such that the worst case gate delay is equal to that of the basic inverter. Assume that the basic inverter has  $(W/L)_N=1.2 \ \mu m/0.5 \ \mu m$  and  $(W/L)_P=3 \ \mu m/0.5 \ \mu m$ . What is the total area of this gate if channel lengths  $L_N$  and  $L_P$  are the same as that of the basic inverter, i.e.  $L_N=L_P=0.5 \ \mu m$ .



Fig. 2: Pull-down section of the CMOS logic gate

**9)** Read the **Displaying Voltage Transfer Characteristics with VEE** section in **Experiment 2**. Bring the **Experiment 2 manual** with you when you come to the laboratory.

# **III. Experimental Work**

#### a) CMOS Inverter

**1)** Fig. 3 shows the schematic view of a CMOS inverter. Construct this circuit by using CD4007 MOS array chip as shown in Fig. 3. Connect pin 14 to  $V_{DD}$ =5 V and pin 7 to ground.



Fig. 3: The schematic view of a CMOS inverter and CD4007 pin diagram

- 2) Connect the multimeter in current measuring mode between  $V_{DD}$  and pin 11. Connect the input to 0V and 5V and determine the power dissipation of the circuit in each case. Comment on the result. Does the CMOS inverter dissipate static power? Explain your reasoning.
- **3)** Obtain the voltage transfer characteristics of the CMOS inverter with the help of VEE. Set  $V_{DD}$ =5 V. Sweep the  $V_{IN}$  from 0 V to 5 V in 0.05 V steps.
- **4)** Find the critical voltages, **V**<sub>IL</sub>, **V**<sub>IH</sub>, **V**<sub>OL</sub>, **V**<sub>OH</sub>, **V**<sub>M</sub> and **noise margins**. Are the low noise margin and the high noise margin near to each other? Is CMOS a good inverter in this respect?

- 5) Connect a **100pF capacitor between** the **output** and **ground**. Change the waveform at the function generator to a **square wave** of **10 kHz**. Connect a **1 k\Omega resistor between pin 9** and **ground**. Connect **Channel 1** of the scope to the **input** and **Channel 2** to **pin 9** and observe the voltages on the scope. Comment on the voltage waveform on the resistor which also represents the current waveform during switching.
- 6) In this part, we will display the dynamic power dissipation of the CMOS inverter as the frequency is varied. For this purpose, we will measure average current with the multimeter. Connect the multimeter between  $V_{DD}$  and pin 11 for current measurement.

 $\rightarrow$  Since there are two types of function generator in the laboratory and IVI drivers do not exist for Agilent 33120A, we will use different VEE configurations for them.

# i) Configuration for Agilent 33120A Using Plug & Play Drivers

- From **Instrument Manager**, click on **HP33120A** and then **PNP** button and place the **Plug & Play Driver** in the work area.
- Click on the driver and change its title as **"function generator"** from the **Properties** menu at the left side of the work area.
- Double click on the <Double-Click to Add Operation> bar of the driver. Select High Level Control → Apply Commands → Apply Command Setup. From the Panel tab, select Square as func, 5 as ampl and 0 as offs. Click on Configuration tab. Under freq, choose Parameter Value as Variable and click on Create Input Terminal. Click OK.
- Double click on the <Double-Click to Add Operation> bar of the driver. Select Low Level Control → Output Configuration Commands → Output Voltage Offset Setup. From the Panel tab, select 2.5 as voltOffs.
- From **Instrument Manager**, click on **HP34401A** and **IVI** button to create IVI-COM Driver Object. Place the driver in the work area.
- Change the title of the driver object as **multimeter**.
- Double click on the **<Double-Click to Add Operation>** bar of the **multimeter**. Select **CreateInstance** and Click **OK**. Click **OK** in the opened **Edit "CreateInstance"** window.
- Double click on the **<Double-Click to Add Operation>** bar of the **multimeter**. Select **Initialize** and Click **OK**. Enter **simulate=false** into the **OptionString** field and click **OK**.
- Double click on the **<Double-Click to Add Operation>** bar of the **multimeter**. Select **DCCurrent** → **Configure** and Click **OK**.
- Double click on the **<Double-Click to Add Operation>** bar of the **multimeter**. Select **Measurement** →**Read** and click **OK**.
- Enter **100** into the **MaxTimeMilliseconds** area and click **OK**.
- Double click on the **<Double-Click to Add Operation>** bar of the **multimeter**. Select **Close** and click **OK** in the opened window.

• Complete the configuration as shown in Fig. 4.



Fig. 4: Final VEE configuration for Agilent 33120A

# ii) Configuration for Agilent 33320A Using IVI Drivers

- From **Instrument Manager**, click on **HP33220A** and then **IVI** button and place the **IVI Driver** in the work area.
- Click on the driver and change its title as **"function generator"** from the **Properties** menu at the left side of the work area.
- Double click on the **<Double-Click to Add Operation>** bar of the driver. Select **CreateInstance** and Click **OK**. Click **OK** in the opened **Edit "CreateInstance"** window.
- Double click on the **<Double-Click to Add Operation>** bar of the driver. Select **Initialize** and Click **OK**. Set **Reset** value to **False** from the drop-down menu and click **OK**.
- Double click on the <Double-Click to Add Operation> bar of the driver. Select Apply →SetSquare and Click OK. From Edit Parameters tab, enter 5 as Amplitude and 2.5 as Offset. Click on Configure Terminals tab. Under Frequency, click on Variable and Create Input Terminal. Click OK.
- Double click on the **<Double-Click to Add Operation>** bar of the driver. Select **Close** and click **OK** in the opened window.
- From **Instrument Manager**, click on **HP34401A** and **IVI** button to create IVI-COM Driver Object. Place the driver in the work area.
- Change the title of the driver object as **multimeter**.
- Double click on the **<Double-Click to Add Operation>** bar of the **multimeter**. Select **CreateInstance** and Click **OK**. Click **OK** in the opened **Edit "CreateInstance"** window.
- Double click on the **<Double-Click to Add Operation>** bar of the **multimeter**. Select **Initialize** and Click **OK**. Enter **simulate=false** into the **OptionString** field and click **OK**.
- Double click on the **<Double-Click to Add Operation>** bar of the **multimeter**. Select **DCCurrent** → **Configure** and Click **OK**.
- Double click on the **<Double-Click to Add Operation>** bar of the **multimeter**. Select **Measurement** →**Read** and click **OK**.

- Enter **100** into the **MaxTimeMilliseconds** area and click **OK**.
- Double click on the **<Double-Click to Add Operation>** bar of the **multimeter**. Select **Close** and click **OK** in the opened window.
- Complete the configuration as shown in Fig. 5.



Fig. 5: Final VEE configuration for Agilent 33220A

- **7)** Using this configuration, we will sweep the frequency of the input square wave from 10 kHz to 100 kHz with 10 kHz steps. We will display the dissipated power versus frequency.
- **8)** Make sure that **100 pF capacitor** is **still connected** between the output and ground. Run the VEE program and comment on the **frequency dependence** of the power dissipation in CMOS circuits.
- **9)** Now, connect **another 100 pF capacitor** between output and ground. In this way, load capacitance is equal to **200 pF**. Run the VEE program again. Compare the results with those obtained in part 8. Comment on the effect of **load capacitor**.

#### b) CMOS Logic Gates

**1)** Fig. 6 shows the pin diagram of 74HC00 IC (2-input CMOS NAND). Insert 74HC00 IC into your breadboard. Connect pin 14 to 5 V and pin 7 to ground. Leave the other pins unconnected and measure the voltages on pins 1,2,3,4,5,6,8,9,10,11,12, and 13. Comment on the results. Is it a good idea to leave the **unused pins unconnected** in CMOS NAND gates?



Fig. 6: The pin diagram of 74HC00 IC

- **2)** Now use one of the NAND gates in the IC. Short circuit the two inputs. Set  $V_{DD}$  to 5V. Connect a **100 pF capacitor** between the output and ground and measure the **rise** and **fall** times. Comment on the result.
- **3)** Construct the 3-input CMOS NAND gate you designed in the Preliminary Work. Obtain the truth table of this gate. **Be careful with using CD4007 MOS chip. Some NMOS and PMOS transistors are connected to each other internally. Use more than one CD4007 if needed.**
- **4)** Construct the CMOS logic circuit that realizes the function **Y=A'+B'D'+C'D'** using 8 transistors. Obtain its truth table.