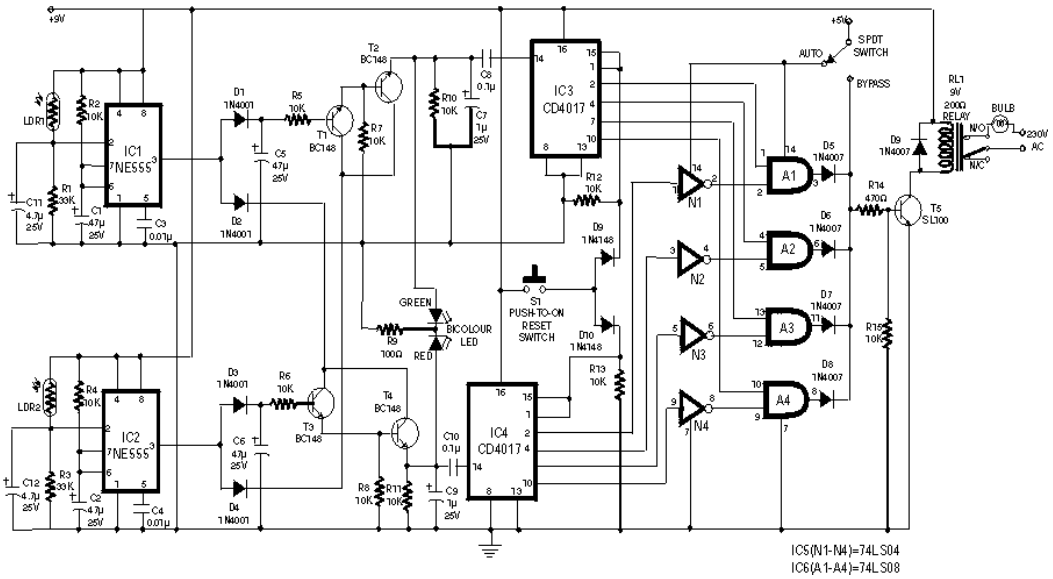
EE312 DIGITAL ELECTRONICS LECTURE NOTES

by Assoc.Prof. Barış Bayram

Spring 2014-2015 (rev.3)



Prepared by

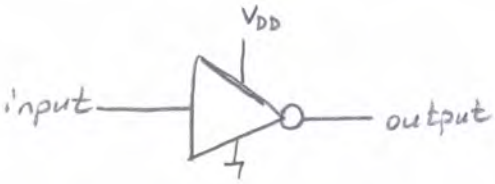
Göktuğ Cihan ÖZMEN

Digital Blocks

Buffer

It seperates input and output
(protection)

Inverter

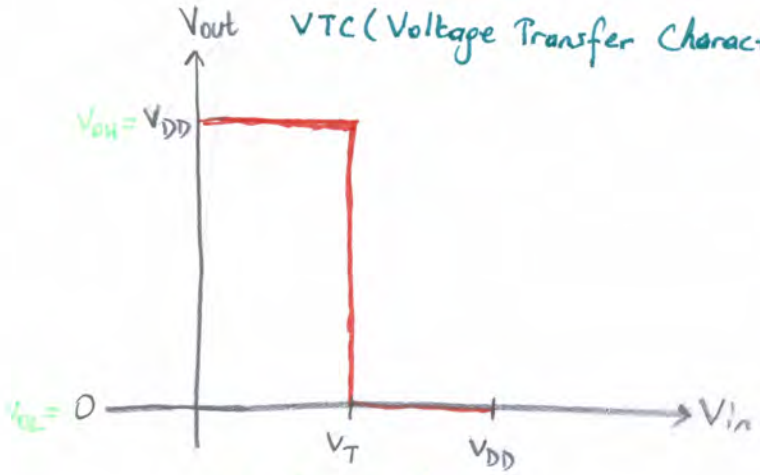


If the input is A, output will be $\bar{A}$
(logic operation)

☆ V_{DD} input V_{DD} output

0V 0V

VTC (Voltage Transfer Characteristics)



$V_T = V_{IL} = V_{IH} = \frac{V_{DD}}{2}$

(ideal inverter)

V_{OH} : Output High Voltage
V_{OL} : Output Low Voltage
V_{IH} : Input High Voltage
V_{IL} : Input Low Voltage
V_T : Treshold Voltage

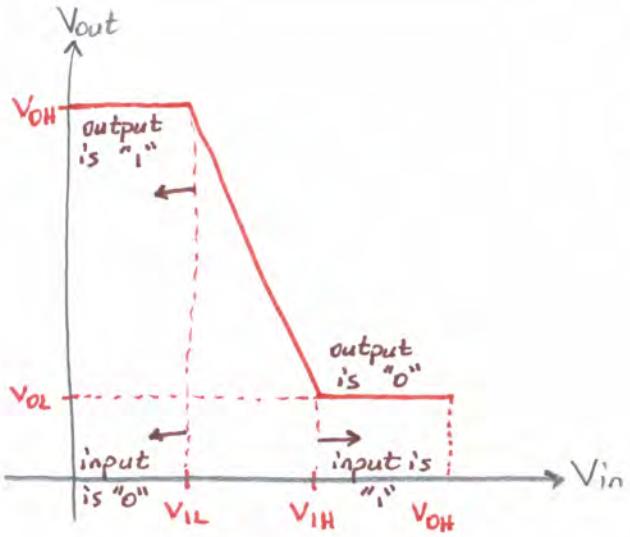
☆ For an ideal inverter,

if $V_{in} < \frac{V_{DD}}{2} \Rightarrow V_{out} = V_{DD}$

if $V_{in} > \frac{V_{DD}}{2} \Rightarrow V_{out} = 0$

if $V_{in} = \frac{V_{DD}}{2} \Rightarrow$ indeterminate

☆ For practical cases (non-ideal cases), the following VTC is obtained, in general.



If $V_{in} < V_{IL} \Rightarrow V_{in}$: "0" (L)

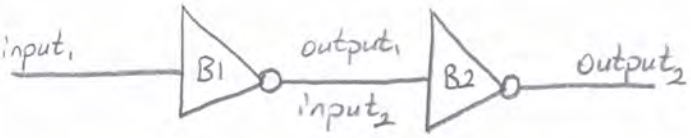
If $V_{in} > V_{IH} \Rightarrow V_{in}$: "1" (H)

☆ Transition width: The amount of voltage change that is required of the input voltage to cause a change in the output state.

$$V_{TW} = V_{IH} - V_{IL}$$

☆ Larger $V_{TW} \Rightarrow$ transition is taking longer amount of time.

☆



B1 and B2 are identical.

What is the requirement for compatibility?

Let $V_{OL} = 0.5V$, $V_{OH} = 5V$, $V_{IL} = 1.5V$, $V_{IH} = 3V$, $V_{DD} = 5V$

$input_1$: "0" $\Rightarrow input_1 = V_{OL} = 0.5V$

$\Rightarrow output_1 = V_{OH} = 5V \Rightarrow output_1$: "1"

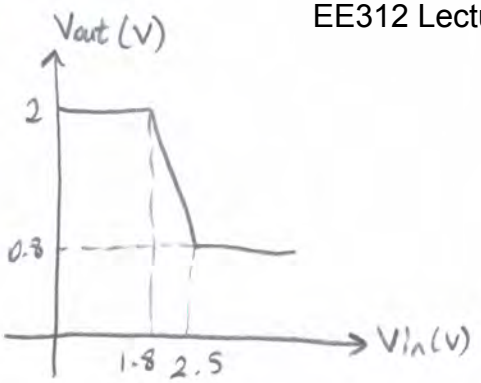
$\Rightarrow input_2$: "1" $\Rightarrow input_2 = V_{OH} = 5V$

$\Rightarrow output_2 = V_{OL} = 0.5V \Rightarrow output_2$: "0"

Hence, we need the following conditions:

$$V_{OL} < V_{IL}$$
$$V_{OH} > V_{IH}$$

Ex:



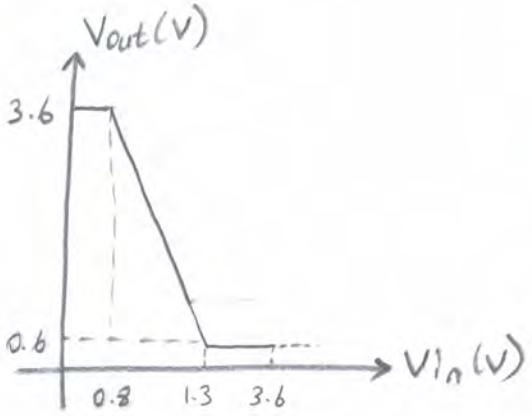
Determine whether it is compatible or not.

$V_{OL} = 0.8V$, $V_{IL} = 1.8V$ } $V_{OL} \leq V_{IL}$ ✓

$V_{OH} = 2V$, $V_{IH} = 2.5V$ } $V_{OH} \not\geq V_{IH}$ ✗

So, this is the VTC of an inverter which is not compatible

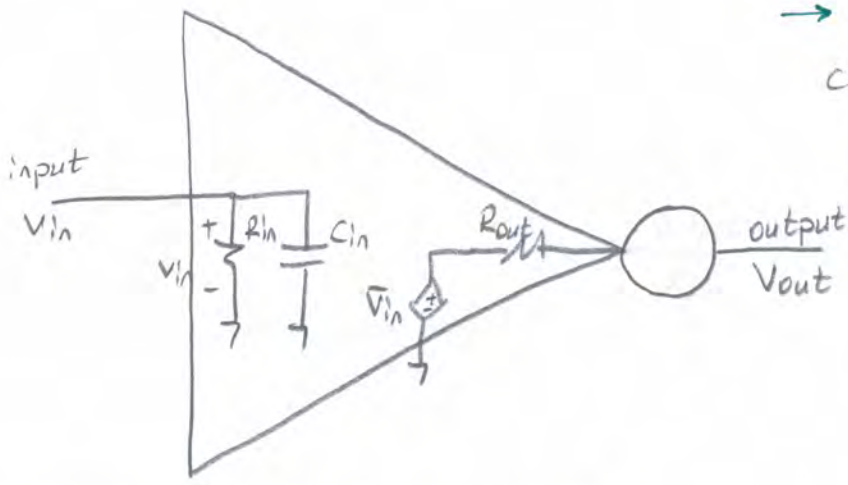
☆ Let $V_{DD} = 5V$.



On VTC, Vin does not extend through V_{DD}, but instead, it extends up until V_{OH}. The reason is that in cascaded cases, the maximum possible input voltage is V_{OH}.

☆

→ VTC is a static characteristics.



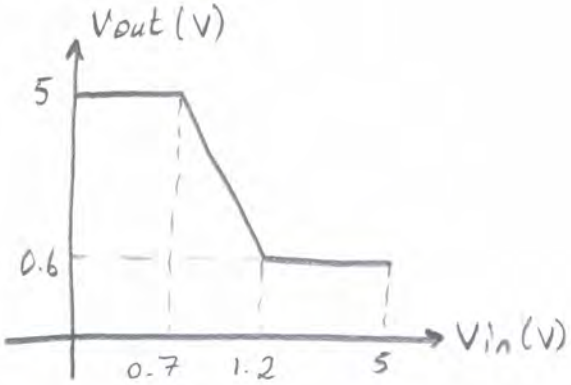
→ VTC is independent from the value of Cin.

(internal structure of an inverter)

→ VTC is obtained when the output is open-circuited.

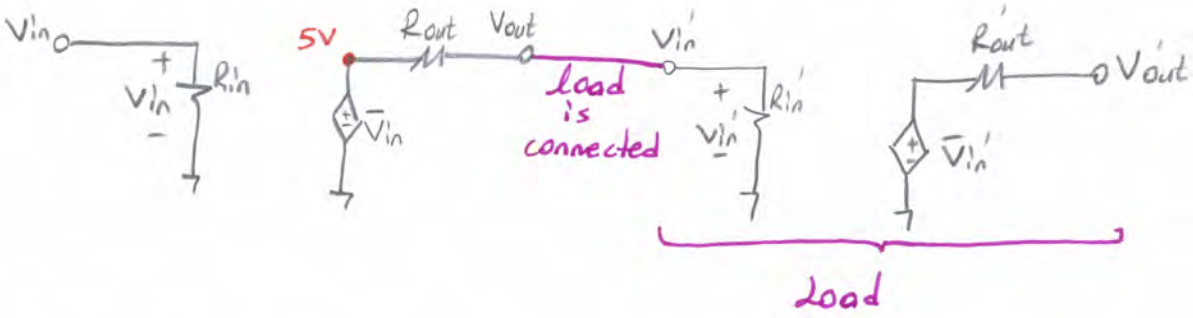
Since VTC is a static characteristics, connecting a capacitor at the output does not affect VTC

Ex: Consider the internal structure of an inverter. Let two inverters are connected in cascaded. Also, let $V_{in} < V_{IL}$ and consider the following VTC for both of them.



Let $R_{in} = R_{in}' = 9k\Omega$

$R_{out} = R_{out}' = 1k\Omega$



$$V_{out} = \frac{5}{R_{out} + R_{in}'} R_{in}' \Rightarrow V_{out} = 4.5V \Rightarrow V_{in}' = 4.5V \Rightarrow \text{input': "1"}$$

$\Rightarrow$ output' = "0"

→ Now assume parallel loads are connected.

$$V_{out} = \frac{5}{R_{out} + \frac{R_{in}'}{N}} \left(\frac{R_{in}'}{N}\right), \text{ For proper operation, } V_{out} = V_{in}' > 1.2V.$$

$\Rightarrow N < 28.5 \Rightarrow \boxed{N = 28}$ $\Rightarrow$ this is the maximum # of parallel connections can be performed to obtain digital "1". In fact, this is the fanout of the inverter.

Noise Margin

It is defined for logical "1" and for logical "0" as follows:

$NMH = V_{OH} - V_{IH} > 0$: noise margin high

$NML = V_{IL} - V_{OL} > 0$: noise margin low

Ex: What are the values of $V_{OL}, V_{IL}, V_{OH}, V_{IH}$ for the maximum noise margin?

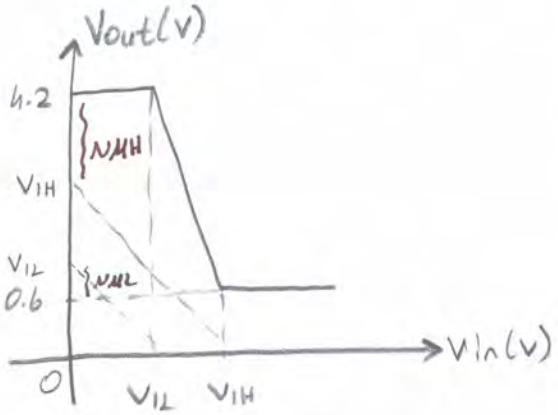
$V_{OL} = 0$
$V_{IL} = 2.5V$
$V_{OH} = 5V$
$V_{IH} = 2.5V$

$NMH = 5 - 2.5 = 2.5V$
$NML = 2.5 - 0 = 2.5V$

In fact, this is the ideal inverter VTC case.

Ex: $V_{DD} = 5V, V_{OL} = 0.6V, V_{OH} = 4.2V$. What are the conditions for maximum fanout?

$\underbrace{V_{IL} - V_{OL}}_{NML} = \underbrace{V_{OH} - V_{IH}}_{NMH}$ if the circuit is not given.



$NML = NMH = \frac{4.2 - 0.6}{2} = 1.8V$

So, $V_{IL} = 2.4V, V_{IH} = 2.4V$

Ex: Now assume that $K_n = \frac{\mu_n C_{ox}}{2}\frac{W}{L} = 1\,mA/V^2$, $V_{DD} = 5V$, $V_{OL} = 1V$, $V_{OH} = 4V$. Find the maximum fanout, V_{IL}, V_{IH}.

Assume $V_{in} = 1V$. $\Rightarrow V_{IL} = 1V$ (maximum voltage that can be achieved at the output of first inverter. - no load case.)

$NML = V_{IL} - V_{OL} = 0V$ ✓

As # of loads increases, Vout decreases.

So, as # of loads increases, the inverter become more stable.

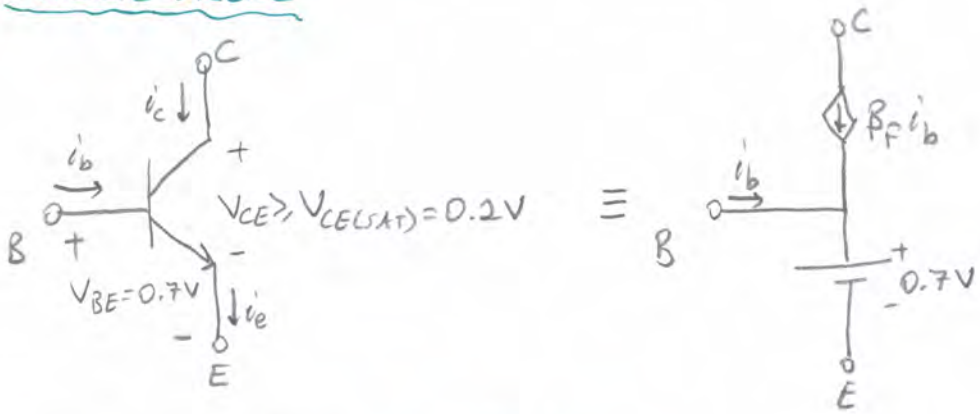
Choose $V_{IH} = 1V$ for maximum noise margin.

$\therefore V_{IH} = V_{IL} = 1V$, maximum fanout $\rightarrow \infty$

Bipolar Junction Transistor (BJT)

BJT has 4 regions of operations; namely, forward active (F.A.), reverse active (R.A.), saturation (SAT), cut-off (OFF)

Forward Active

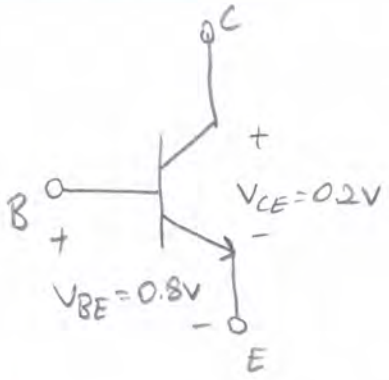


Conditions for F.A. Region:

1. $\frac{i_c}{i_b} = \beta_F$
2. $V_{BE(on)} = 0.7V$
3. $V_{CE} \geq$

Remark: For digital design, BJTs with $\beta_F = 20\text{-}30$ are preferred.

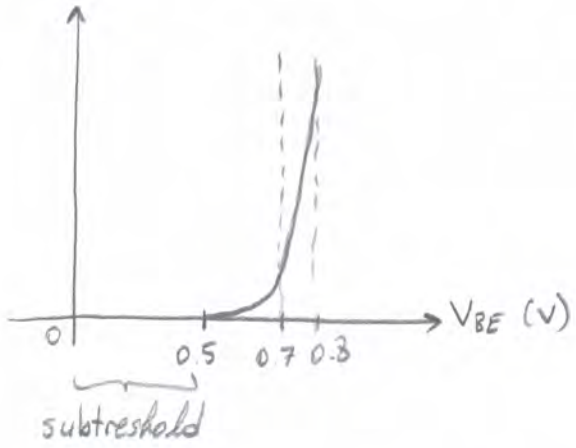
Saturation



Conditions for SAT Region:

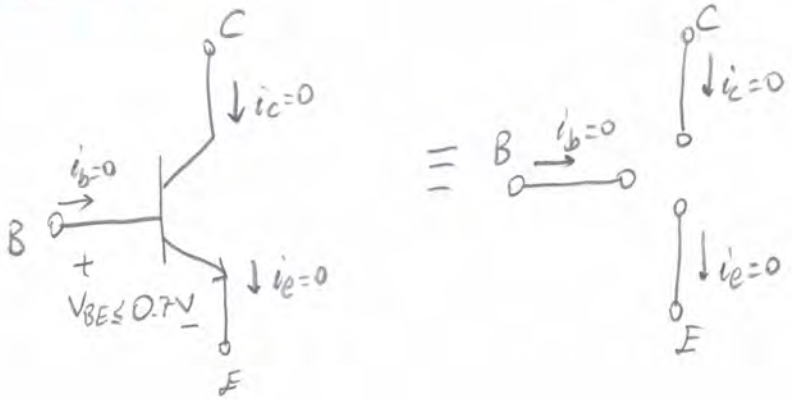
1. $i_c/i_b \leq \beta_F$
2. $V_{CE} = 0.2V$
3. $V_{BE} = 0.8V$

★ Transition from F.A. Region to SAT Region is smooth.



Since we have exponential characteristics, starting from very low current values, in F.A. Mode, $V_{BE} = 0.7$ is assumed. However; for SAT Region, V_{BE} is assumed to be equal to 0.8V and the change between F.A. and SAT is due to the exponential characteristics.

Cut-Off



Conditions for OFF Mode:

1. $V_{BE} \leq 0.7V$
2. $i_b = 0$
3. $i_c = 0$

Ex: The following BJTs are identical and in different circuits.

($\beta_F = 20$, $i_b = 10\mu A$ for all of them.)

	BJT_1	BJT_2	BJT_3	BJT_4
i_c(mA)	0	0.1	0.15	0.25

Find the operating regions of all transistors.

BJT_1 → cut-off (since $i_c = 0$ and in that case i_b become 0A)

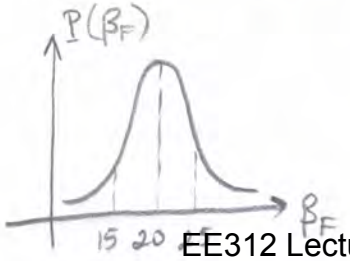
★ We have C_π and C_μ capacitances in BJT. They cause a phenomenan called transition time. If the transition time is large, then this BJT is called deeply saturated. If the transition time is small, this BJT is called lightly saturated.

BJT_2 → deeply saturated. (if F.A. → $i_c = 0.2mA$ and the difference between 0.2mA and 0.1mA is large, so the transition time is large)

BJT_3 → lightly saturated.

BJT_4 → forward active

In BJT's β_F value varies with some percantage.

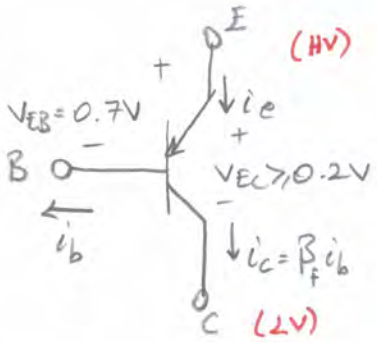


In some cases, we have even 50% variation in β_F.

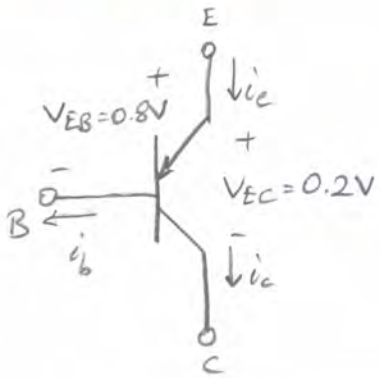
Since $\frac{i_c}{i_b} > \beta_F$, we cannot say it is in SAT, we say that it operates in F.A. Region.

pnp BJT

Forward Active

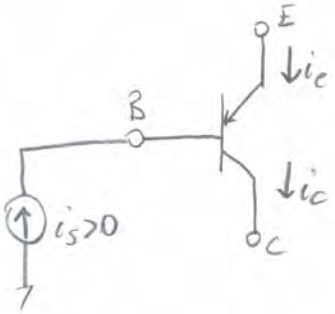


Saturation



$i_c \leq \beta_f i_b$

OFF



In this case $i_b = 0$

$\Rightarrow i_c = i_e = 0$

$\Rightarrow$ cut-off

★ In fact, in this case, the transistor will break out.

★ For a pnp transistor, we have the following measurement results:

$V_{EB} = 0.8V$

$V_{EC} = 0.2V$

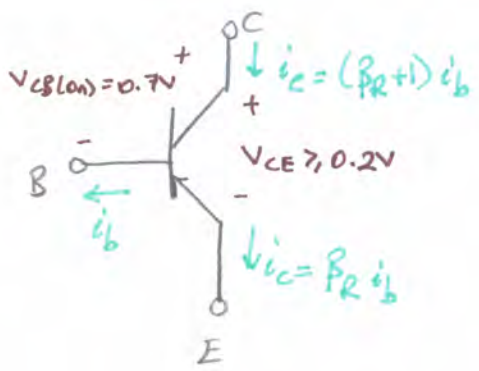
$i_e = 0$ ($i_b = i_c = 0$)

Determine the region of operation.

Since $V_{EB} > 0.7V$, the operation region is SAT.

In fact, the transistor can operate in SAT if it is excited by a current, but no current flows through the transistor.

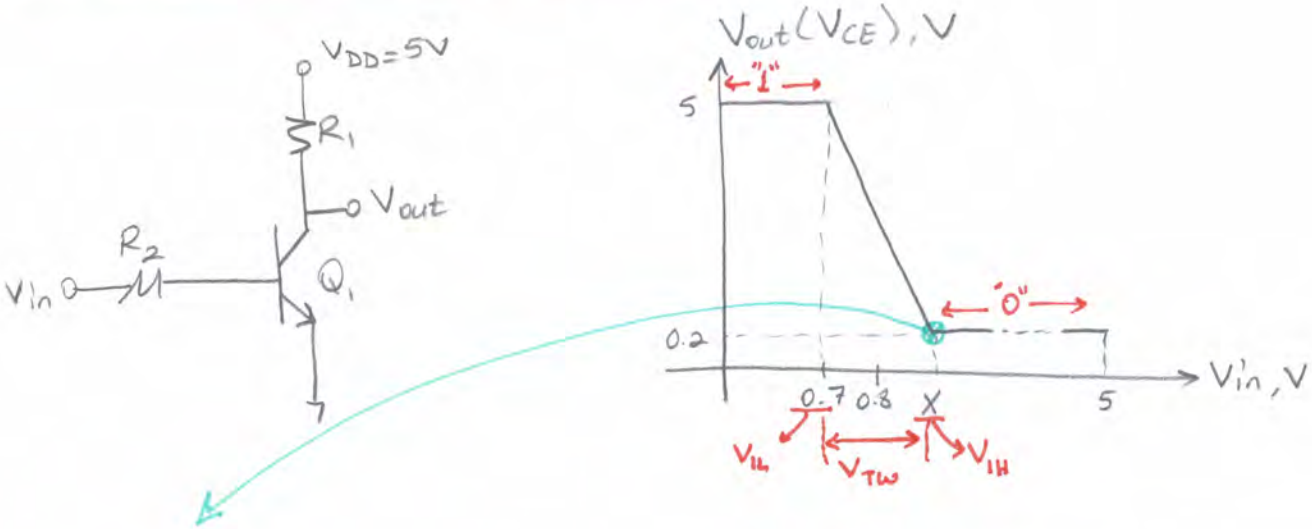
Reverse Active



In reverse active mode, emitter behaves as if it were collector and vice versa.

($\beta_R = 0.5$ in general)

Resistor Transistor Logic (RTL)



$$i_c = \frac{V_{DD} - V_{CE(sat)}}{R_1}, \quad i_b = \frac{i_c}{\beta_F}$$

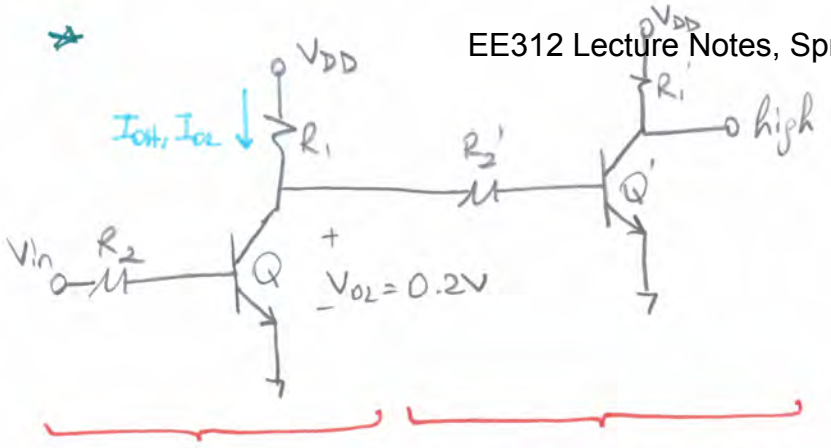
$$V_{in} = 0.8 + R_2 i_b = 0.8 + \frac{1}{\beta_F}\frac{R_2}{R_1}(5 - 0.2) = 0.8 + \frac{1}{\beta_F}\frac{R_2}{R_1}(4.8)$$

$$V_{IH} = V_x = V_{in}' = 0.8 + \frac{1}{\beta_F}\frac{R_2}{R_1}4.8$$

Ex: $V_{IH} \leq 1.2V$, $0.1 \leq \frac{R_1}{R_2} \leq 10$, $\beta_F = 20$, $\beta_R = 0.5$. For those conditions, determine V_{IH} with V_{TW} minimum.

$$V_{IH} = 0.8 + \frac{1}{20}\frac{R_2}{R_1}4.8 = 0.8 + 0.24\frac{R_2}{R_1}, \quad \text{Let } \frac{R_2}{R_1} = 0.1, \frac{R_1}{R_2} = 10$$

$$\Rightarrow \boxed{V_{IH} = 0.8024V, \ \frac{R_1}{R_2} = 10}$$



$$P_{OH} = V_{DD} I_{OH}$$

$$P_{OL} = V_{DD} I_{OL}$$

$$P_{av} = \frac{P_{OH} + P_{OL}}{2}$$

? Does P_{OL} depend on the # of gates?

No, since in OL case, loads will be in cut-off and no current can flow through them and the only parameter that describes I_{OL} will be the operation mode of Q.

★ For $NML\ (= V_{IL} - V_{OL})$, what is the maximum fanout in OL case?

It is $N \to \infty$ since loads will not be driven anyway.

★ For V_{OH}, when load is connected to the output of Q, VTC will become out of consideration.

V_{OH} with 1 load is: $V_{OH_1} = \frac{(5-0.8)}{R_1+R_2} R_2 + 0.8$

(Since, for V_{OH}, Q is in OFF, current will not flow through Q)

→ Now let, $R_1 = 10k\Omega, R_2 = 40k\Omega \Rightarrow V_{OH1} = 4.16V > V_{IH}$, so acceptable. ✓

★ If N loads are connected:

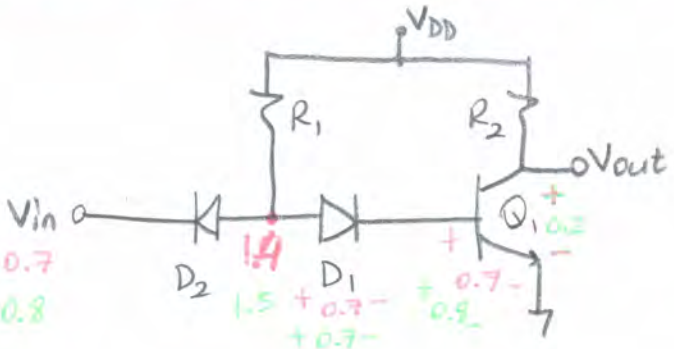
$$V_{OHN} = \frac{(5-0.8)}{10k + \frac{40k}{N}} \frac{40k}{N} + 0.8 \geq 1.76V \text{ for proper operation.}$$

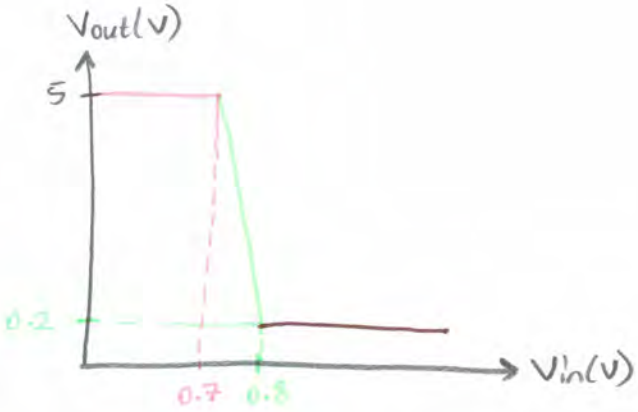
$\Rightarrow N \leq 13.5 \Rightarrow \boxed{N = 13}$ maximum # of fanout.

(For V_{IH}, $V_{out} = V_{CE} = 0.2V \Rightarrow i_C = 0.48mA \Rightarrow V_{IN} = 0.8 + \frac{i_C}{\beta_F} \cdot 40k = 1.76V$)

V_{OL}

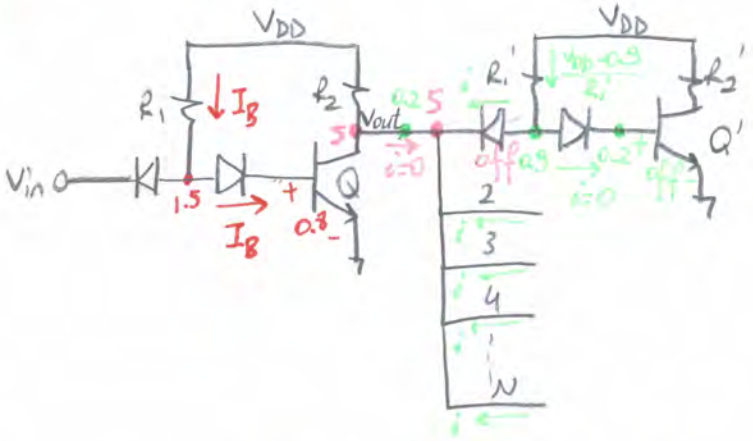
Diode-Transistor Logic (DTL)





★ In RTL, maximum fanout is limited. As a result, we try our chance with DTL.

★



→ For output high case, since the diode shown above cannot be on, no current can flow through the loads. As a result, maximum fanout is infinite.

→ For output low case, in order Q to be in SAT, $I_C \leq \beta_F I_B$. Also, we should consider NML.

$$NML \geq 0 \Rightarrow V_{IL} - V_{OL} = 0.7 - 0.2 = 0.5 \geq 0$$

V_{OL} can increase up to 0.7V

★ In fact, β_F varies a lot, so we use a parameter called saturation parameter to guarantee ourselves.

$$I_C = \left(\frac{5-0.2}{R_2} + N \frac{5-0.9}{R_1} \right), \quad I_B = \frac{5-1.5}{R_1}$$

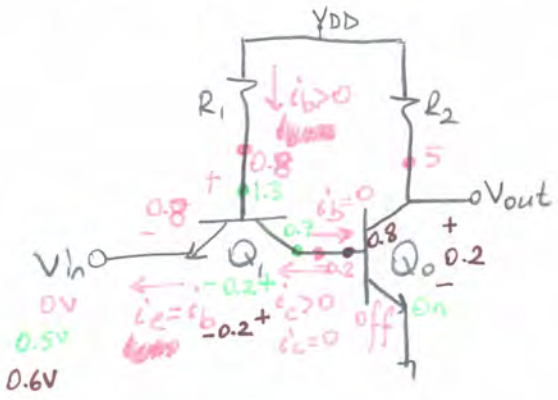
$$I_C \leq \sigma_0 \beta_F I_B \Rightarrow \boxed{\frac{(4.8)}{R_2} + \frac{N(4.1)}{R_1} \leq \sigma_0 \beta_F \frac{(3.5)}{R_1}}$$

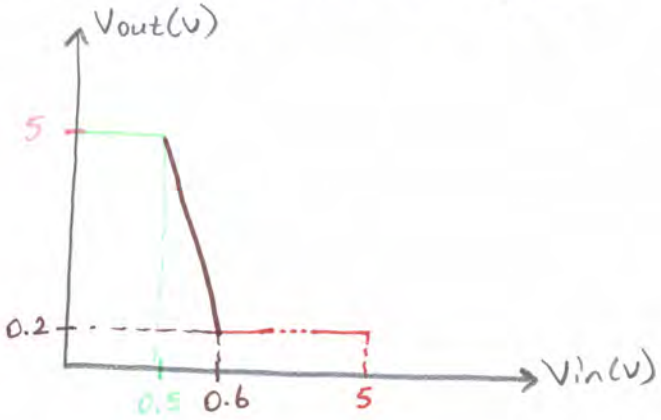
$\sigma_0 \sim 0.8$, $\beta_F \sim 20$

★ We observed that [illegible] for DTL.

Transistor - Transistor Logic (TTL)

In DTL, we have two back-to-back diodes which looks like a transistor. We, now, try to find VTC of TTL which contains two BJTs.



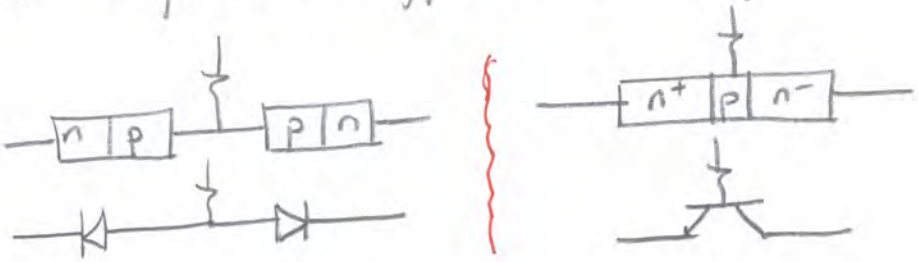


★ For output-high case, $i_e = i_b$, Q_1 is in SAT, $i_c = 0$. For a transistor be in SAT, $i_c \le \beta_F i_b \Rightarrow$ this is obviously satisfied, but we clearly see that Q_1 is deeply saturated. In fact, we make use of the saturation parameter to get intuition about the level of saturation of a transistor.

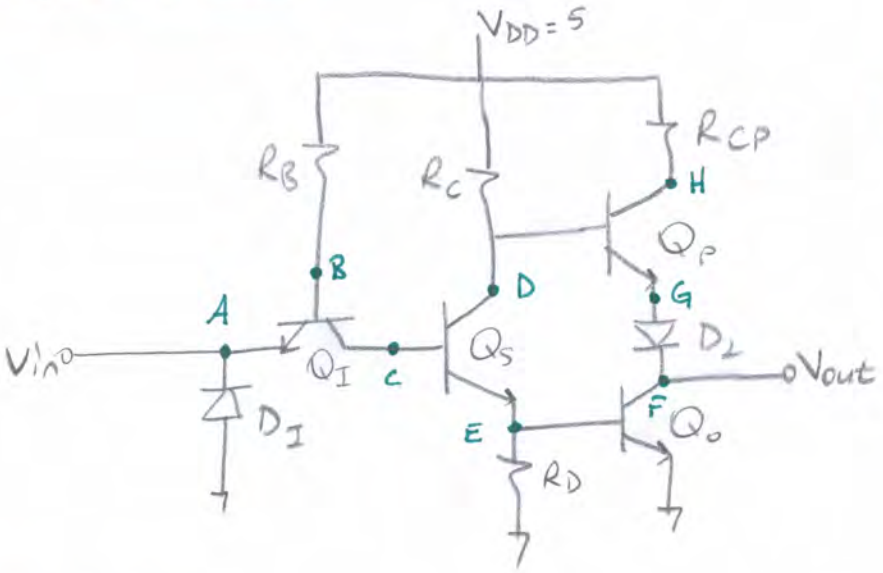
if σ_0 is large $\Rightarrow$ lightly saturated $\left(i_c = \sigma_0 \beta_F i_b\right)$

if σ_0 is small $\Rightarrow$ deeply saturated $\left(\sigma_0 \le 1\right)$

★ V_{IL} of TTL is 0.5V. It was 0.7V for DTL case. This difference comes from the fact that in the fabrication of BJT, doping difference is used in order to achive better performence. The most general configuration of that difference is as follows:



Standard TTL



* The points, indicated by capital letters (A, ..., H), represents the voltages at that points.

1. $V_{in}=0$

$V_A=0$, Assume Q_I in SAT.

$V_B=0.8V$, $V_C=0.2V$ $\Rightarrow$ cannot open Q_S. $\Rightarrow$ Q_S is OFF.

Since Q_S is OFF, no current will flow through R_D $\Rightarrow$ $V_E=0$.

So, Q_O is also OFF. $\Rightarrow$ no current flows through Q_O $\Rightarrow$ no current flows through D_L. $\Rightarrow$ no current flow through Q_P.

However, due to voltages at the branches of Q_P, it is clear that it operates in F.A. Region. $V_H=5V$, $V_D=5V$ $\Rightarrow V_G=4.3V$

This satisfies F.A. Region requirements. $\Rightarrow V_{D_L}=0.7V \Rightarrow V_{out}=V_F=3.6V$

2. In order to consider the rest of the circuit, we first need to open Q_S or Q_O. But which opens first?

Q_S turns on first, since Q_S opens at the voltage of $V_C=0.7V$ which makes $V_E=0V \Rightarrow Q_O$ is OFF. In order to have $V_C=0.7V$, we need to have $V_{in}=V_A=0.5V$ since Q_I is still in SAT.

Since Q_O is still OFF, no current flows through it. This causes no current flow through Q_P and it is still in F.A. ($V_H=5V$, $V_{DG}=0.7V$)

3. At what point Q_p opens?

In order to open Q_p, we need to have $V_E = 0.7V \Rightarrow Q_s$ is already open $\Rightarrow V_C = 1.4V \Rightarrow Q_I$ is in SAT $\Rightarrow V_{in} = V_A = 1.2V$

Here comes the question: Q_p or Q_s saturates first?

(Assume $R_C = 1.6k\Omega$, $R_D = 1k\Omega$)

Now, assume Q_p saturates first. $\Rightarrow V_E = 0.8V$ $V_F = 0.2V$

current through R_D is $I_{R_D} = 0.8mA$ (Assume β_F is large for all transistors.)

$I_{R_C} = 0.8mA \Rightarrow V_D = 5 - I_{R_C} R_C = 3.72V \Rightarrow V_G = 0.8V \Rightarrow V_{DG} = V_{BE_{Q_p}} = 2.82V$

which is not possible. $\Rightarrow$ so Q_s saturates first.

After Q_s saturates, $V_D = 0.8V \Rightarrow$ if Q_p were still F.A. $\Rightarrow V_G = 0.2V$

However, Q_p is in F.A. $\Rightarrow V_F > 0.2V \Rightarrow$ so, at some point Q_p becomes OFF. Also, before Q_p becoming OFF, D_2 also becomes OFF.

4. At what point Q_p saturates?

In order to have Q_p in SAT, $V_F = 0.2V$, $V_E = 0.8V$. Q_s is in SAT

$V_{out} = 0.2V$

$\Rightarrow V_C = 1.6V \Rightarrow V_A = V_{in} = 1.4V$

At $V_{in} = 1.8V \Rightarrow Q_p, Q_s$ in SAT, Q_p is OFF, D_2 is OFF

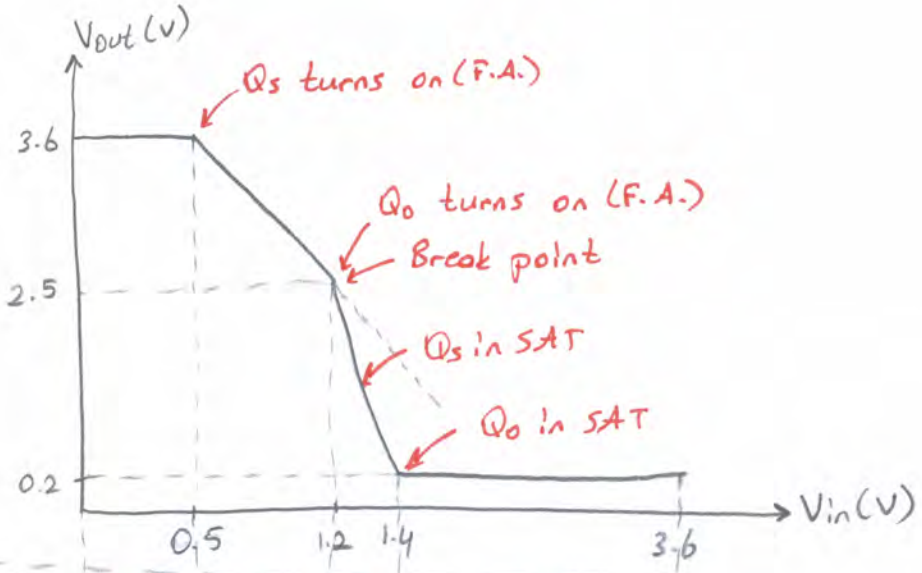
$\Rightarrow V_C = 1.6V \Rightarrow$ which causes Q_I be in R.A. above $V_{in} = V_A > 1.8V$.

★ D_I is used for safety, i.e. protect the circuit if negative voltages are given from V_{in}.

★ Q_s is the decision transistor of this TTL circuit. Q_p is pull-up, Q_p is pull-down transistors and according to V_{in}, Q_s decides which transistor will be open, Q_p or Q_p.

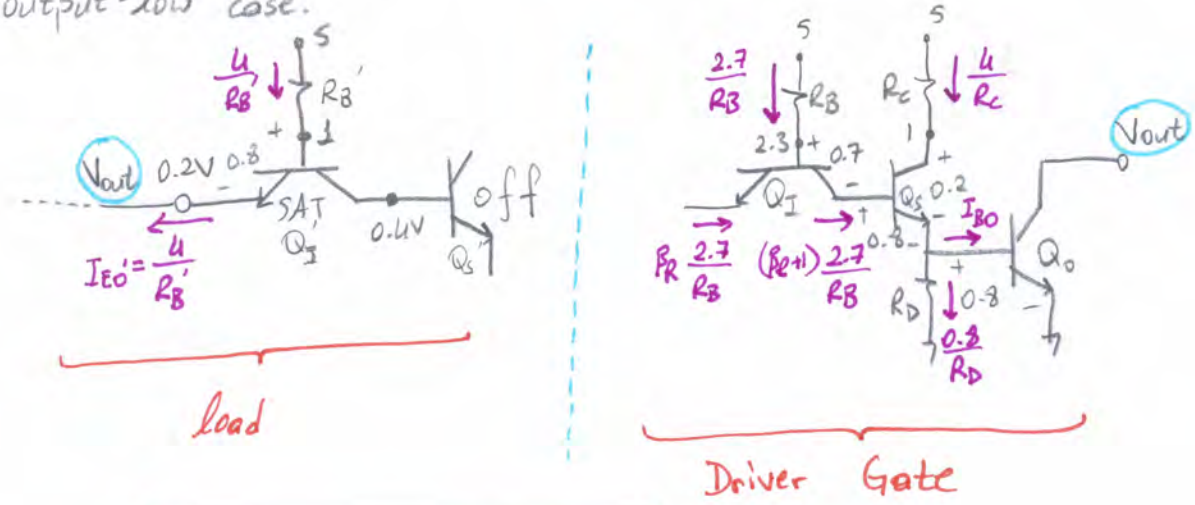
★ Without D_2, at output low case, both Q_p and Q_p will be open and this is the reason why we have D_2 in our circuit.

Now we have all the voltages for standard TTL and we will also indicate the operation regions of all transistors and D_L for all input voltages.



Q_o	OFF	OFF	F.A.	SAT
Q_s	OFF	F.A.	F.A./SAT	SAT
Q_p	F.A.	F.A.	F.A./OFF	OFF
D_L	ON	ON	ON/OFF	OFF
Q_I	SAT	SAT	SAT	SAT/R.A.

Now, we will find the value of maximum fanout. Let's first work on output-low case.



$$I_{BO} = \frac{4}{R_C} + (\beta_F + 1)\frac{2.7}{R_B} - \frac{0.8}{R_D}$$

We have $\sigma_0 = 0.8$

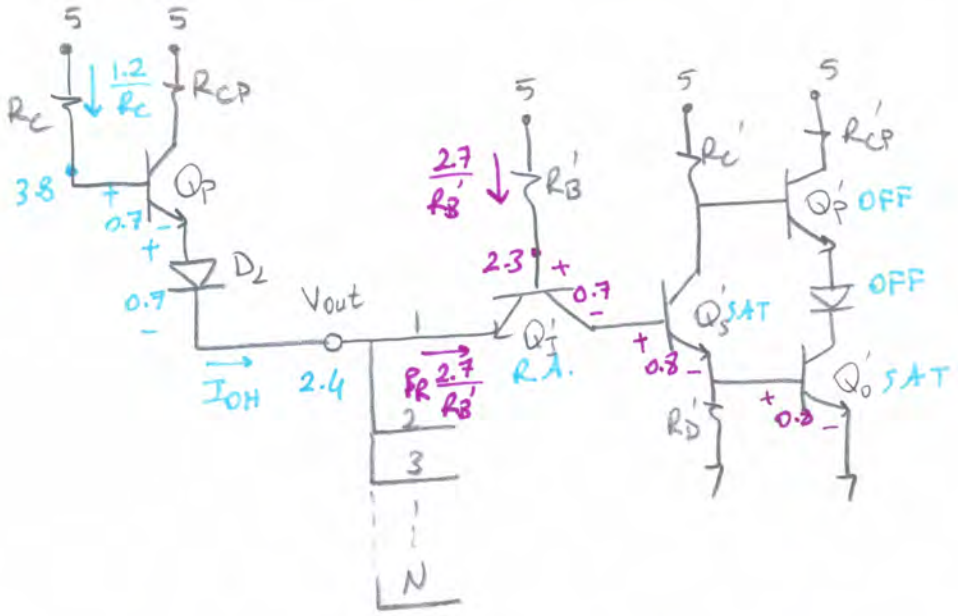
$$\sigma_0 = \frac{I_{comax}}{\beta_F I_B} \Rightarrow I_{comax} = \sigma_0 \beta_F I_{BO}$$

$$I_{comax} = N I_{EO'} = N \frac{4}{R_B'}$$

$$\Rightarrow \boxed{N \frac{4}{R_B'} = \sigma_0 \beta_F \left(\frac{4}{R_C} + (\beta_R + 1) \frac{2.7}{R_B} - \frac{0.8}{R_D} \right)}$$

From this equation, we can find N for OL case.

Now, let's work on output-high case.



We should have $NMH > 0$, but for safety, let's choose $NMH = 1V$

$NMH = V_{OH} - V_{IH} \Rightarrow V_{OH} = 1.4 + 1 = 2.4V$

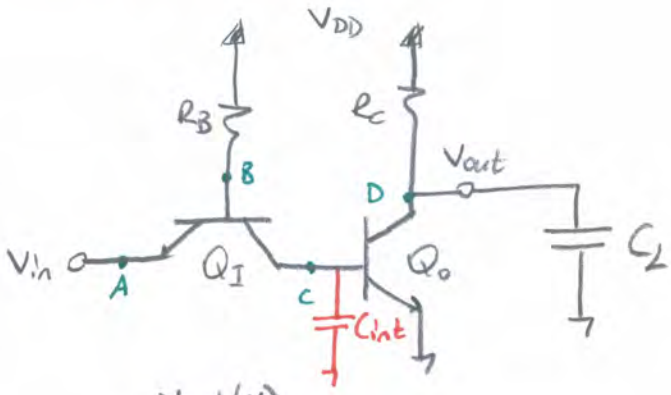
So, $I_{OH} = (1+\beta_F) \frac{1.2}{R_C}$, $I_{OH} = N \beta_R \frac{2.7}{R_B'}$

$$\Rightarrow \boxed{N \beta_R \frac{2.7}{R_B'} = (1+\beta_F) \frac{1.2}{R_C}}$$

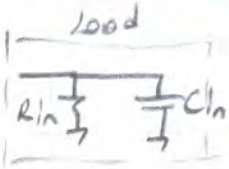
From this equation, we can find N for OH case

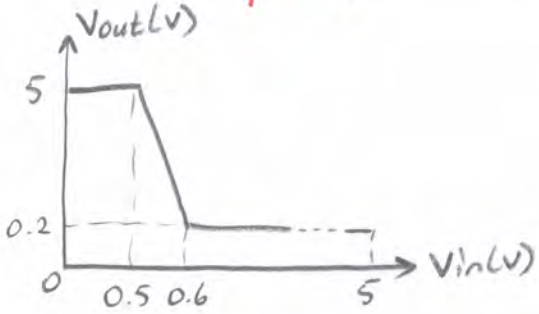
$$\boxed{N = \min(N_{OH}, N_{OL})}$$

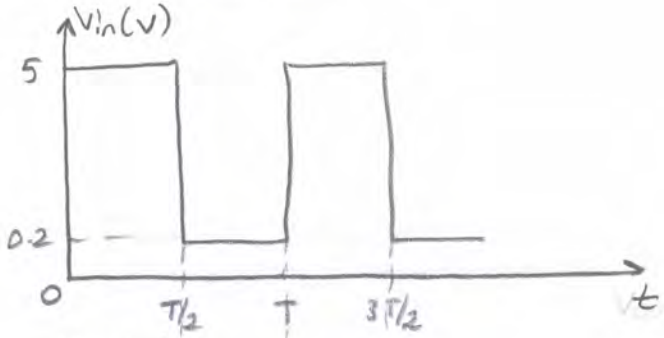
Capacitive Load

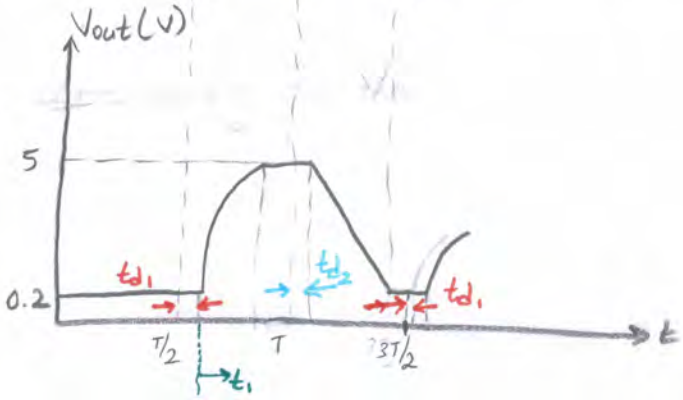


$C_L = NC_{in}$ (for N load case, in parallel)









* We are supposed to find V_{out} corresponding to $V_{in}(t)$ given above.

* Till T/2, $V_{out} = 0.2V$ since given circuit is an inverter and it has the given VTC.

* In the case of $V_{in} = 5V$ (input high), Q_I is in R.A. and Q_O is in SAT. We have C_{int} given in the circuit and this is the internal capacitance of Q_O. It is small, but it can be charged, of course. While $V_{in} = 5V$, $V_C = 0.8V$ since Q_O is in SAT. Now, we are supposed to consider the change in V_{in}. $V_{in} = 0.2V$ results in the change in the operation of Q_I. V_{AC} is no longer greater than 0.2V, in fact $V_{C1} = 0.6V$. This causes Q_I to operate in F.A. region. While C_{int} discharges, Q_O becomes operating in OFF since V_C becomes less than 0.7V. Also, V_C can fall to 0.4V since collector-emitter voltage of Q_I must be 0.2V at least. At that point Q_I becomes operating in SAT.

☆ For a small interval called t_{d_1}, V_{out} stays the same as 0.2V. During this interval C_{int} discharges. This t_{d_1} can be found as follows:

$$\Delta Q_{int} = C_{int}\Delta V = C_{int}(0.8-0.7)$$

$$t_{d_1} = \frac{\Delta Q_{int}}{I_{int}}$$

I_{int} is the current supplied by C_{int} due to the change in V_{in}, resulting in the change in the operation region of Q_1.

Since Q_1 is in F.A, $V_B = 0.9V \Rightarrow I_{BQ_1} = \frac{5-0.9}{R_B}$

$$I_{int} = I_{CQ_1} = \beta_F I_{BQ_1}$$

$$t_{d_1} = \frac{C_{int}(0.8-0.7)}{\beta_F \frac{(5-0.9)}{R_B}}$$

☆ At the point where $V_C = 0.7V$, Q_0 becomes off and as a result at the output C_L becomes charging by V_{DD}. Here, we have an RC circuit and V_{out} has the following time dependent form:

$$V_{out}(t_1) = A - Be^{-t/\tau} \qquad \tau = R_C C_L$$

t_1 starts at $t = \frac{T}{2} + t_{d_1}$, $\Rightarrow \left(t = \frac{T}{2} + t_{d_1} \Leftrightarrow t_1 = 0\right)$

$$\left.\begin{aligned} V_{out}(t_1=0) &= 0.2V \\ V_{out}(t_1 \to \infty) &= 5V \end{aligned}\right\} \quad V_{out}(t_1) = 5 - 4.8e^{-t_1/\tau}$$

According to this wave form, we can draw V_{out} as indicated in the graph in page 18.

(Here, we said that at the point where $V_C = 0.7V$, Q_0 becomes off. This means beyond that point, i.e $V_C < 0.7V$, Q_0 becomes off.)

* Now, we have [illegible] $t=T$. C_L is loaded till $V_{out}=5V$ and at that point Q_I is in SAT and Q_o is off. Also, $V_C=0.4V$ at that moment since C_{int} is charged. When V_{in} becomes 5V, Q_I becomes operating in R.A. since $V_{AC}=4.4V>0.2V$. During this process C_{int} is charging. However, till $V_C=0.7V$, Q_o is off and $V_{out}=5V$. For V_{out} to start falling, it needs a small time interval when C_{int} charges. This time interval is called t_{d_2} and can be found as follows:

$$\Delta Q_{int} = C_{int}(0.7-0.4)$$

$$t_{d_2} = \frac{\Delta Q_{int}}{I_{int}}$$

I_{int} is the current which charges C_{int} and this current is supplied by Q_I.

Since Q_I is in R.A. $V_B = V_C + 0.7 = 1.1V \Rightarrow I_{BQ_I} = \frac{5-1.1}{R_B}$

$$I_{int} = (1+\beta_R) I_{BQ_I}$$

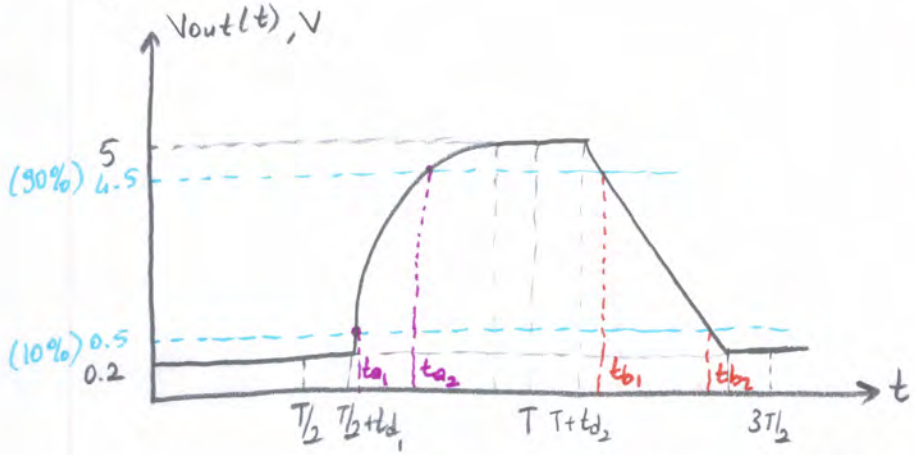
$$t_{d_2} = \frac{C_{int}(0.7-0.4)}{(1+\beta_R)\frac{(5-1.1)}{R_B}}$$

* During t_{d_2}, V_{out} stays the same and it is off. However, after t_{d_2} Q_o becomes operating in F.A. and $V_C=0.7V$. This makes $V_B=1.4V$.

$\Rightarrow I_{BQ_I} = \frac{5-1.4}{R_B} \Rightarrow I_{CQ_I} = I_{BQ_o} = (1+\beta_R) I_{BQ_I}$: this is valid since C_{int} is charged and V_C is fixed as 0.7V and no current flows through it. Since Q_o operates in F.A. C_L starts discharging. At that point we have an assumption.

If $I_{R_C} \ll I_{CQ_1}$, we can neglect I_{R_C} which results in linear behavior in Vout since only C_L discharges. At the point where $V_D = 0.2V$, Q_0 becomes operating in SAT and V_C becomes 0.8V, but this does not affect the circuit. The reason is obvious, Q_1 is still in R.A and Q_I is in SAT.

* Now, we're going to consider Vout(t) again to define the raise time and fall time.

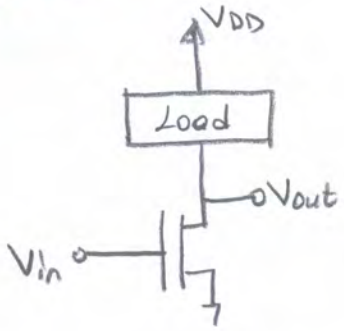


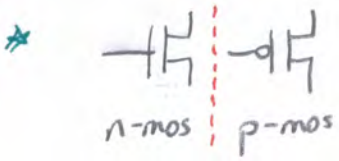
$$t_r = t_{a_2} - t_{a_1}$$
$$t_f = t_{b_2} - t_{b_1}$$

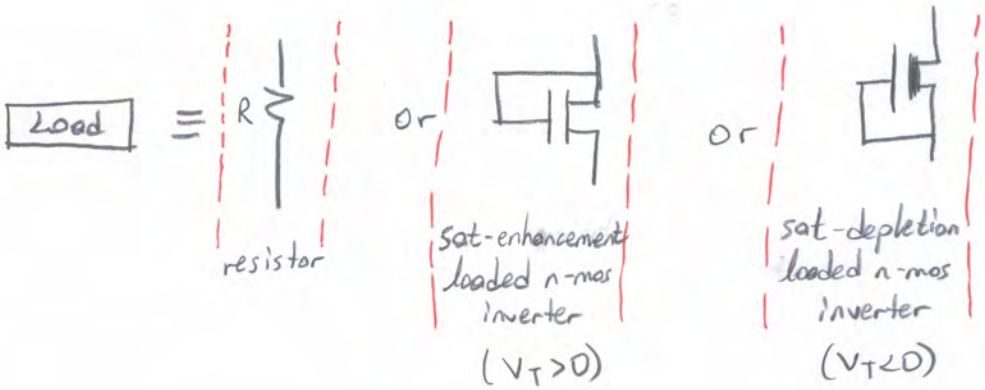
* $t_r > t_f$ since during rising, C_L discharges through resistor; however, during falling, C_L discharges through Q_0. Since transistor operating in F.A. mode is always superior compared to a resistor or any passive element, this statement is valid

$$t_r > t_f$$

NMOS

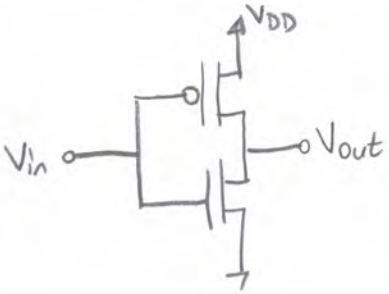




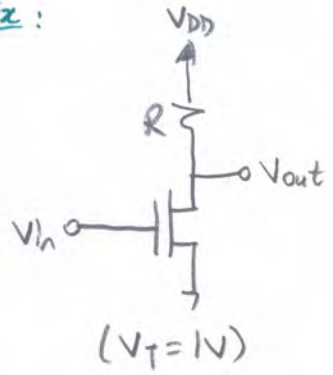


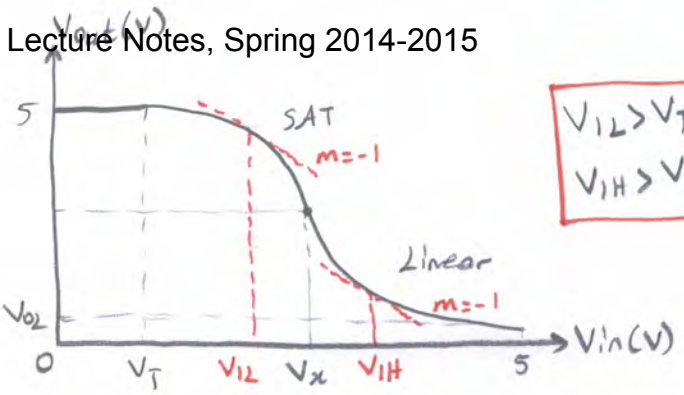
- For nmos:
  - → $V_{GS} < V_T$: OFF, $I_D = 0$
  - → $V_{GS} \geq V_T$: → $V_{DS} \geq V_{GS} - V_T$: SAT
    $$I_D = \frac{1}{2} k_n (V_{GS} - V_T)^2$$
    → $V_{DS} \leq V_{GS} - V_T$: Linear (Triode)

- We have also pmos loaded nmos inverter which is called complementary mos (CMOS).



Ex:





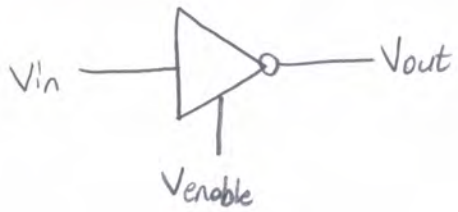
$V_{IL} > V_T$
$V_{IH} > V_{IL}$

* In this case, it is hard to define V_{IL} and V_{IH}. For this reason we consider the points where the slop of VTC is m=-1 and the corresponding input values at those points will be V_{IL} and V_{IH}

* It is clear that $V_{IH} > V_{IL}$ should be satisfied. However, if we solve corresponding equations for input high where nmos is in linear region and we get two solutions both being greater than V_{IL}, we should choose the one which is greater than V_x.

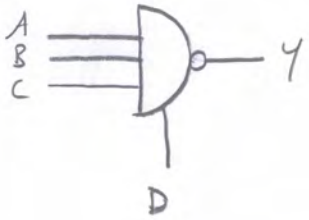
* In fact, on VTC, it is shown that nmos first operates in SAT since at the point just above $V_{in} = 1V$, $V_{GS} > V_T$; I_D starts flowing. However, it is low, so $V_{DS} > V_{GS} - V_T$. However, at some point, $V_{in} = V_x$, V_{DS} becomes less than $V_{GS} - V_T$ and the transistor starts operating in linear region and it does change its operation region by increasing V_{in}.

Tri-State Output



Venable	Vin	Vout
H	L	H
H	H	L
L	L	X
L	H	X

Here, enable signal gives high impedance floating output. This means output behaves like an open circuit when Venable is low. Also, Vout is unspecified in this case.



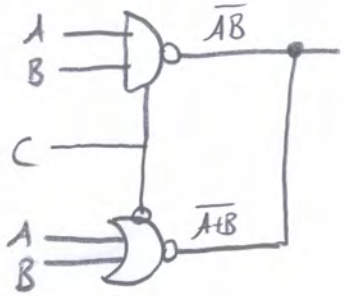
D	A	B	C	Y
1	0	0	0	1
	0	1	0	1
		⋮		
0	-	-	-	X
				X
	-	-	-	X
				X

If D is low, Y will be unspecified, but if D is high, gate will operate properly

* We want to implement a circuit with following conditions:

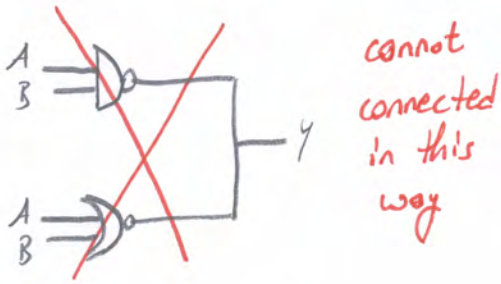
$Y = \overline{AB}$ if $C=1$

$Y = \overline{A+B}$ if $C=0$

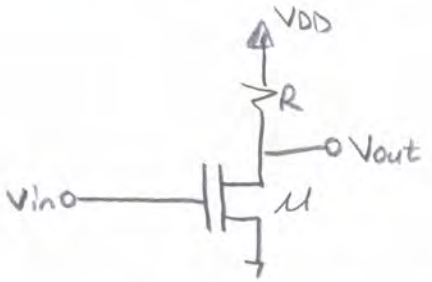


It is possible to implement this, since C is an enable signal and either one of the gates will give an output.

* However, the following configuration is not possible since the same node cannot have both 1 and 0 values.

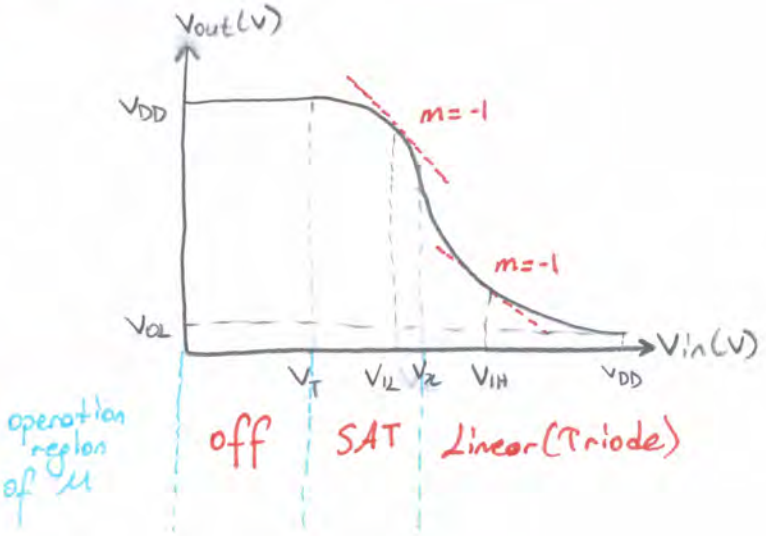


Resistor Loaded N-MOS Inverter (cont'd)



$V_T = 1V,\ K_n = 0.25mA/V^2$

$\lambda = 0$



★ For M being in SAT, we have the followings:

$$I_D = \frac{1}{2} K_n (V_{GS} - V_T)^2 \quad , \quad V_{GS} = V_{in}, \quad V_{DS} = V_{out}$$

$$V_{out} = V_{DD} - R I_D = V_{DD} - \frac{1}{2} R K_n (V_{GS} - V_T)^2$$

$$\frac{dV_{out}}{dV_{in}} = \frac{dV_{out}}{dV_{GS}} = -R K_n (V_{GS} - V_T) \Rightarrow m = -1$$

$$\Rightarrow R K_n (V_{in} - V_T) = 1 \Rightarrow V_{in} = V_T + \frac{1}{R K_n}$$

$$\Rightarrow \boxed{V_{IL} = V_T + \frac{1}{R K_n}}$$

★ Even if V_x is irrelevant for most of the applications, let's consider V_x.

At the point where M changes its operation region ($V_{in} = V_x$), we have

$$V_{GS} - V_T = V_{DS} \Rightarrow V_{out} = V_{in} - V_T = V_{DD} - \frac{1}{2} R K_n (V_{in} - V_T)^2$$

$$\boxed{\frac{R K_n}{2} (V_{in} - V_T)^2 + (V_{in} - V_T) - V_{DD} = 0}$$

Solve for $V_{in} - V_T$ and find $V_{in} = V_x$.

We will have V_{in_1}, V_{in_2} and we'll choose the one which satisfies the following conditions: $\boxed{V_x > V_T,\ V_x > V_{IL}}$

★ For M being in linear region we have the followings:

$$I_D = K_n\left[(V_{GS}-V_T)V_{DS} - \frac{V_{DS}^2}{2}\right], \quad V_{DS} = V_{DD} - I_D R$$

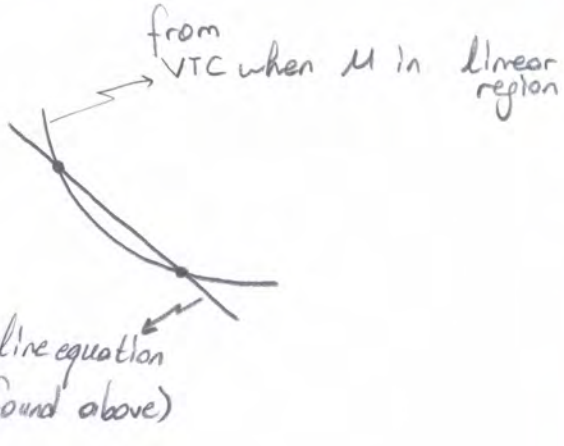
$$V_{DS} = V_{out}, \quad V_{GS} = V_{in}$$

$$V_{out} = V_{DD} - K_n R\left[(V_{in}-V_T)V_{out} - \frac{V_{out}^2}{2}\right], \quad \frac{V_{DD}-V_{out}}{RK_n} = (V_{in}-V_T)V_{out} - \frac{V_{out}^2}{2}$$

In order to find V_{IH}, we should consider $\frac{dV_{out}}{dV_{in}} = -1$

$$\Rightarrow \frac{1}{RK_n} = V_T + V_{out} - V_{in} + V_{out} \Rightarrow \boxed{V_{out} = \frac{V_{in}}{2} - \left(\frac{V_T}{2} + \frac{1}{2RK_n}\right)}$$

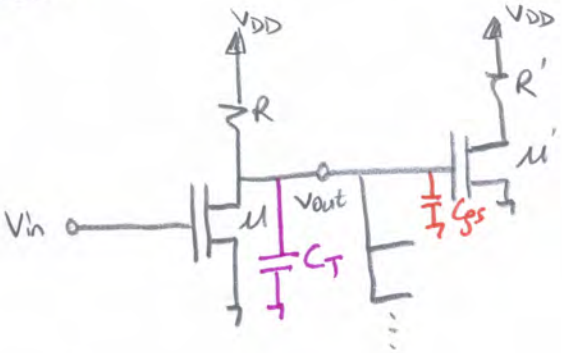
this is a line equation on VTC plane.



It is clear that we have two solutions and we choose the one which satisfies the following conditions:

$$\boxed{\begin{aligned} V_{IH} &> V_{IL} \\ V_{IH} &> V_T \\ V_{IH} &< V_{IL} \end{aligned}}$$

★ Now consider the fanout calculation for the resistor loaded nmos inverter.



→ Consider OH case: $V_{out} = 5V$

$\Rightarrow V_{GS}' > V_T \Rightarrow$ no limit for fanout

$\Rightarrow N_{OH} \to \infty$

→ Consider OL case: $V_{out} < V_T$

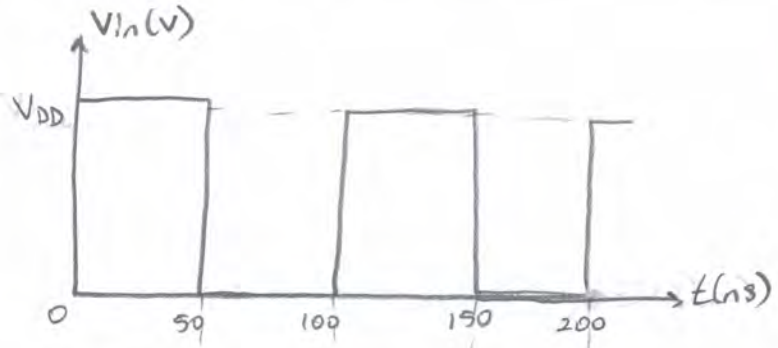
$\Rightarrow M'$ is off $\Rightarrow N_{OL} \to \infty$

$\therefore N \to \infty$

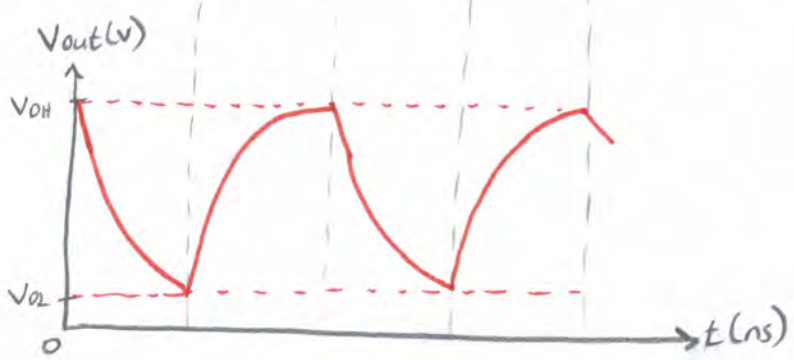
However, this is not the case due to rise time, fall time issues. We have the capacitances illisturated on the circuit above.

$$\boxed{C_T = NC_{gs}}$$

* Suppose that we have the following input waveform with 50% duty cycle and $f_{max} = 10MHz$. ($T = 100ns$)



→ If 30% duty cycle were given, we would say that input has 30ns high, 70ns low voltage in one period.



* First consider the transition from V_{OH} to $V_{OL} \Rightarrow V_{DS} = V_{OH} = V_{DD}$

$\Rightarrow V_{in} = V_{DD} \Rightarrow M$ in SAT ($V_{GS} - V_T = V_{in} - V_T = V_{DD} - V_T \leq V_{DS} = V_{DD}$ ✓)

$\Rightarrow I_D = \frac{1}{2} k_n (V_{GS} - V_T)^2 \Rightarrow V_{GS} = V_{in} = V_{DD}$ (constant) $\Rightarrow$ so I_D constant

$\Rightarrow$ so linear characteristics on Vout vs t graph.

* At some point we will have $V_{DS} \leq V_{GS} - V_T \Rightarrow M$ becomes operating in linear region. $\Rightarrow$ we will have exponential characteristics on Vout vs t graph.

(Neglect I_R since $I_R \ll I_D$.)

$$t_f = \frac{\Delta Q_{C_T}}{I_{C_T}}, \quad I_{C_T} = I_D \text{ in our case.}$$

$$\Delta Q_{C_T} = N_1 C_{gs} (V_{OH} - V_{OL})$$

$\Rightarrow t_f \leq 50ns$ since if this is not the case, this means Vout cannot decrease up to V_{OL} which means our logic is not operating properly.

* So, we have the limit for N1 by looking the discharge of C_T;

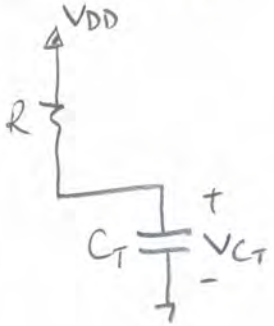
$$N_1 \leq \frac{50\left(\frac{1}{2}K_n(V_{GS}-V_T)^2\right)}{(V_{OH}-V_{OL})C_{gs}}$$

→ If it is said that take the average value of I_D: ($I_{Dfinal} \sim 0$)

$$I_D = \frac{I_{Dinitial} + I_{Dfinal}}{2}$$

$$\Rightarrow I_D = \frac{I_{Dinitial}}{2}$$

* Now consider the transition from V_{OL} to V_{OH} case. We will have an RC circuit with R at the drain of M and C_T. M is operating in off since it is excited by approximately 0V.



$$V_{C_T}(0^-) \equiv 0V$$

⇒ we have an exponential increase with

$$\tau = RC_T = RC_{gs}N_2$$

* So, what is the limit for N_2? In fact, we should have the following condition to obtain V_{OH} when $\Delta t = 50ns$:

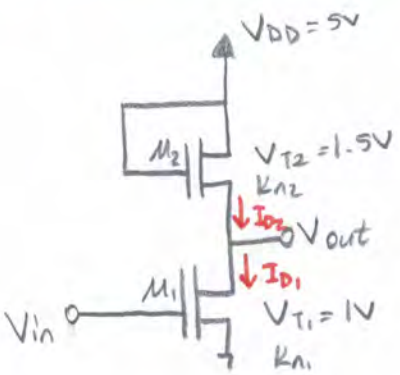
$$5\tau \leq 50ns \Rightarrow \tau \leq 10ns$$

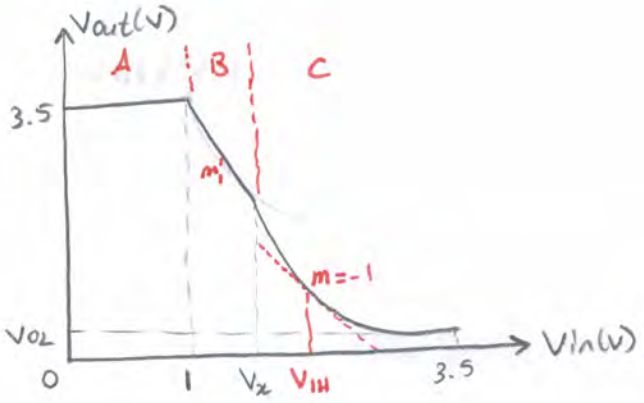
$$\Rightarrow N_2 \leq \frac{10\times10^{-9}}{RC_{gs}}$$

* So, we are done and we can draw Vout as in page 27. Also, maximum fanout can be found as follows:

$$N = \min(N_1, N_2)$$

SAT Enhancement Loaded NMOS Inverter





★ Until $V_{in}=V_{T1}=1V$, M_1 will be off and $V_{DS_2} \geq V_{GS_2}-V_T$ ✓ so M_2 is in SAT ⇒ so, $V_{out}=3.5V$.

★ After $V_{in}=1V$, M_1 becomes operating in SAT.

$$I_{D1}=I_{D2}$$

$$I_{D1}=\frac{1}{2}K_{n1}(V_{GS_1}-V_{T1})^2=\frac{1}{2}K_{n1}(V_{in}-V_{T1})^2$$

$$I_{D2}=\frac{1}{2}K_{n2}(V_{GS_2}-V_{T2})^2=\frac{1}{2}K_{n2}(V_{DD}-V_{out}-V_{T2})^2$$

$$\Rightarrow K_{n1}(V_{in}-V_{T1})^2=K_{n2}(V_{DD}-V_{out}-V_{T2})^2$$

$$\Rightarrow \boxed{V_{out}=-\sqrt{\frac{K_{n1}}{K_{n2}}}(V_{in}-V_{T1})+V_{DD}-V_{T2}}$$

line equation on VTC of the inverter.

★ Operation regions of M_1 and M_2 are as follows:

	A	B	C
M_1	off	SAT	linear
M_2	SAT	SAT	SAT

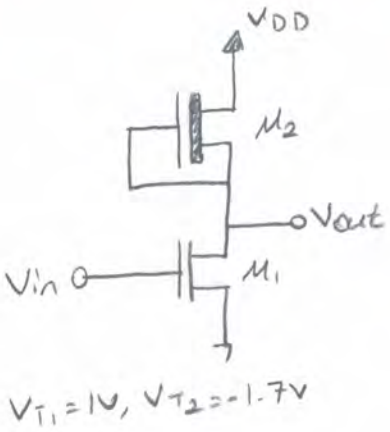
★ Above V_x, M_1 starts operating in linear region resulting in exponential characteristics. (as in the case of resistor loaded nmos inverter.)

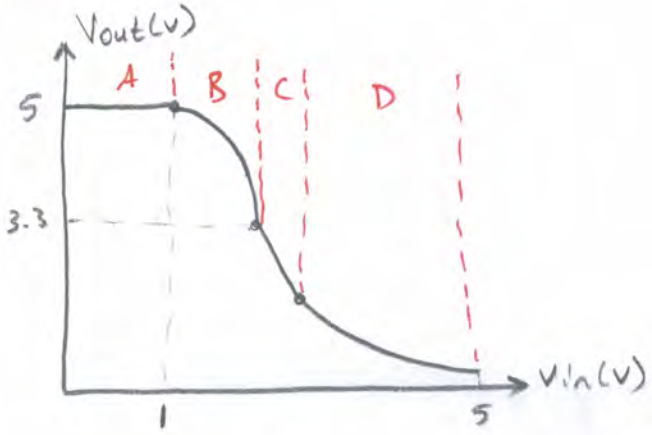
★ If $|m_1|>1 \Rightarrow$ we'll find $V_{IL}=V_{T1}$ (since no point on the graph having $m=-1$ slope when M_1 operates in SAT)

★ If $|m_1|<1 \Rightarrow$ we'll not have any V_{IL} i.e. V_{IL} does not exist.

★ If $m_1=-1 \Rightarrow$ we'll have $V_{IL}=V_{T1}$ and since starting from V_x till 3.5V we have exponential characteristics, slope will no longer be -1 when M_1 operates in linear region. (slope continuously decreases in magnitude)

SAT Depletion Loaded N-MOS Inverter





★ Until $V_{in}=V_{T1}=1V$, M_1 will be off. $V_{GS_2}=0>V_{T2}V$ M_2 is on. $I_{D_1}=0$ $\Rightarrow I_{D_2}=0 \Rightarrow$ since $V_{GS_2}-V_{T_2}=1.7V\neq 0$, M_2 cannot operate in SAT. So, M_2 operates in linear region. $I_{D_2}=K_n\left((V_{GS_2}-V_{T_2})V_{DS_2}-\frac{V_{DS_2}^2}{2}\right)$. The only way for obtaining $I_{D_2}=0$ is setting $V_{DS_2}=0 \Rightarrow V_{out}=5V$.

★ After $V_{in}=1V$, M_1 starts operating in SAT. At the point where $V_b=3.3V$, M_2 starts operating in SAT. With increasing V_{in}, at some point M_1 starts operating in linear region.

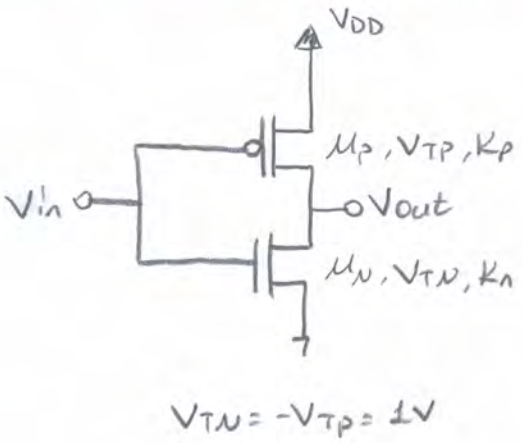
✱ Operation regions of M_1 and M_2 are as follows:

	A	B	C	D
M_1	off	SAT	SAT	linear
M_2	linear	linear	SAT	SAT

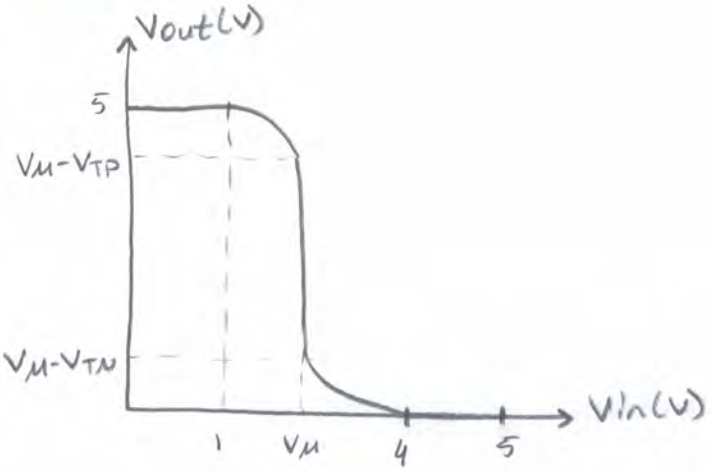
✱ If we are to consider resistor loaded, sat enhancement loaded and sat depletion loaded nmos inverters, transition widths of them can be compared as follows:

$$TW_{resistor} > TW_{sat\ enhancement} > TW_{sat\ depletion}$$

Complementary MOS (CMOS) Inverter



$V_{TN} = -V_{TP} = 1V$



✱ When $V_{in} < V_{TN}$, M_N is off. $V_{SGp} > 1V \Rightarrow I_{D_N} = 0 \Rightarrow I_{Dp} = 0$, $V_{GS} - V_{TP} \neq 0$ so, M_p cannot operate in SAT $\Rightarrow$ M_p is in linear region. At the point $V_{in} = V_{TN} = 1V$, M_N becomes operating in SAT. At some point, $V_{in} = V_M$, M_p starts operating in SAT. Let's find V_M.

$$I_{D_N} = \frac{1}{2} K_n (V_M - V_{TN})^2, \quad I_{Dp} = \frac{1}{2} K_p (V_{DD} - V_M + V_{TP})^2, \quad I_{DN} = I_{DP}$$

$$\Rightarrow \boxed{V_M = \frac{V_{DD} + V_{TN}\sqrt{\frac{K_n}{K_p}} + V_{TP}}{1 + \sqrt{\frac{K_n}{K_p}}}}$$

✱ At V_M since both M_N and M_P are in SAT, Vout sharply decreases and at some Vout value M_N becomes operating in linear region. When $V_{in}=4V$, M_P becomes off since $V_{SG} < |V_{TP}|$ above that input.

✱ Now, assume we want $V_M = \frac{V_{DD}}{2}$. For that purpose consider V_M.

$$V_M = \frac{V_{DD} + V_{TP} + V_{TN}\sqrt{\frac{K_n}{K_p}}}{1+\sqrt{\frac{K_n}{K_p}}} = \frac{V_{DD}}{2}$$

if $V_{TP} = -V_{TN}$ and $K_n = K_p \Rightarrow$ we can achieve our objective.

✱ Consider two end points of V_M line. At the top, M_P becomes operating in SAT which means: $V_{SD_P} = V_{SG_P} + V_{TP}$

$$\Rightarrow 5 - V_{out} = (5 - 2.5) - 1$$

$$V_{out} = 3.5V \Rightarrow \boxed{V_{out} = V_M - V_{TP}}$$

Now consider the bottom of V_M line, M_N starts operating in linear region, resulting in the following:

$$V_{DS_N} = V_{GS_N} - V_{TN} \Rightarrow \boxed{V_{out} = V_M - V_{TN}}$$

✱ V_{IH} and V_{IL} will be found as before: consider the points where $m=-1$ and find corresponding input voltage values for them. We will find V_{IL} and V_{IH} by this method.

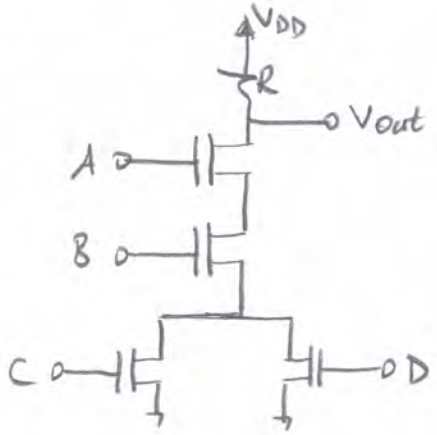
✱ Also notice that, During $V_{in} = V_M$, the transition in the output voltage equals to $V_{TN} - V_{TP}$.

Ex: Consider the following logic function:

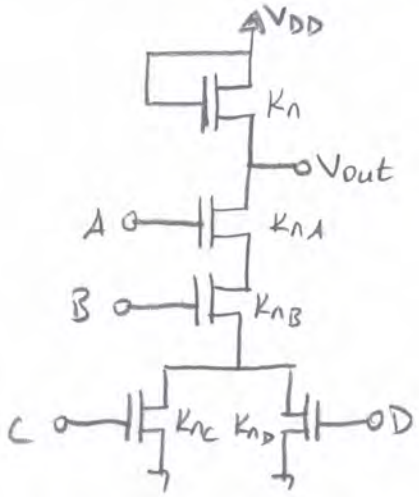
$$Y = \overline{AB(C+D)}$$

Implement this function by using

a. Resistor loaded nmos inverter.



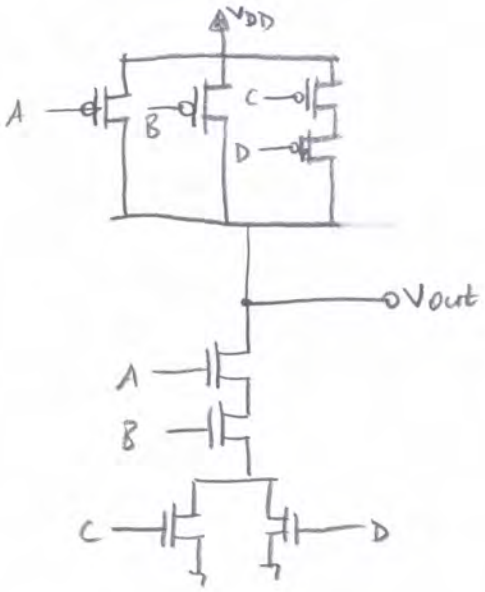
b. SAT enhancement mode nmos inverter.



Let $K_{nA} = K_{nB} = K_{nC} = K_{nD} = 1mA/V^2$. Which value of K_n is most suitable for the design? $K_n = 1mA/V^2$, $K_n = 0.1mA/V^2$, $K_n = 10mA/V^2$.

We want that while pull-up is turned on, pull-down is turned of and vice versa. For large K_n, both pull-up and pull-down will be on which is undesired. So, choose K_n as small as possible.

$$K_n = 0.1mA/V^2$$ ✓

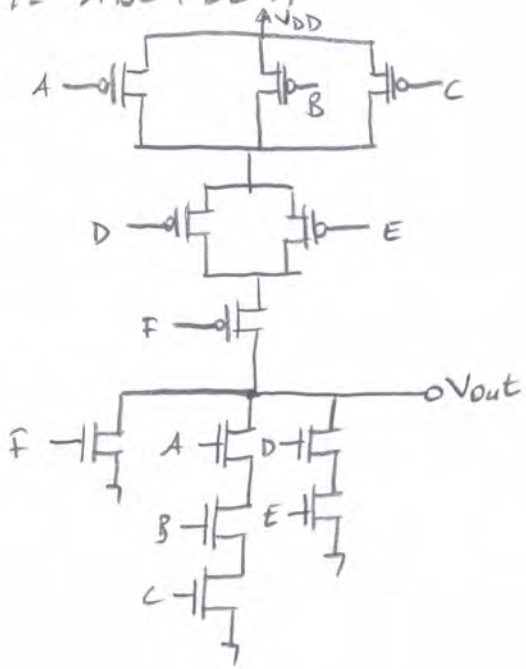


By using CMOS Inverter,

we can achieve zero output voltage.

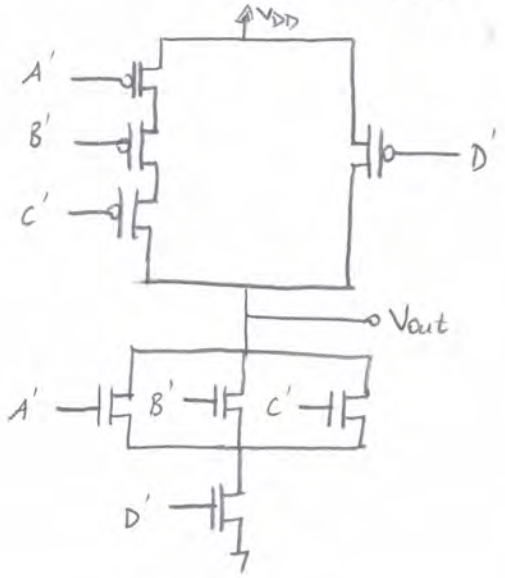
Ex: Implement the following logic function by CMOS Inverter.

$Y = \overline{ABC + DE + F}$

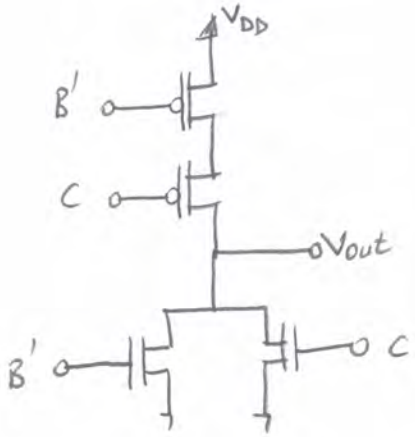


Ex: $Y = ABC + D$

$$Y = \overline{\overline{ABC + D}} = \overline{(A' + B' + C')D'}$$



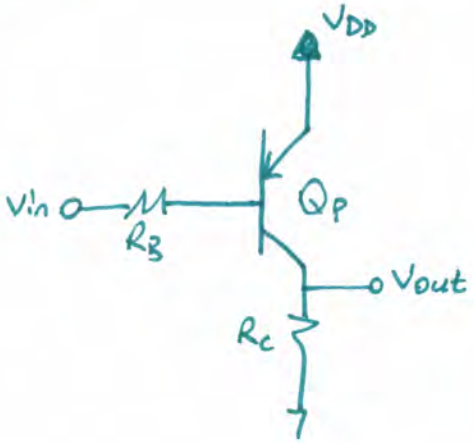
Ex: $Y = \overline{A'B(C+A) + B'+C} = \overline{A'BC + B'+C} = \overline{B'+C(A'B+1)} = \overline{B'+C}$



if complements of inputs are available, we need 4 transistors to implement this function. However; if not, we need one more transistor for B' (inverter) which makes the number of transistors 5.

EE312 MIDTERM I QUESTIONS

Q.1.



$\beta_F = 20$

$\beta_R = 0.5$

$|V_{BE(F.A.)}| = 0.7V$

$|V_{BE(SAT)}| = 0.8V$

$|V_{CE(SAT)}| = 0.2V$

$R_B = 10k\Omega$

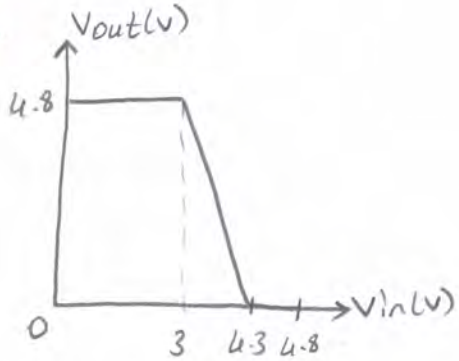
$R_C = 2k\Omega$

$V_{DD} = 5V$

a. Sketch the VTC of this inverter. Find the values of $V_{OH}, V_{OL}, V_{IH}, V_{IL}$.

b. Calculate the power dissipation of this gate when it is driving one similar gate.

a.



First, Q_P is in SAT: $V_{out} = 5 - 0.2 = 4.8V$.

At some point, it starts operating in F.A.R. Let's find this point:

$5 - V_{in} = 0.8 + I_B R_B$

$\beta_F I_B R_C = 4.8 \Rightarrow I_B = 0.12mA$

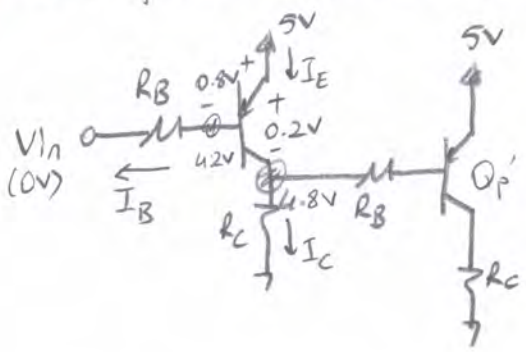
$\Rightarrow V_{IL} = 5 - 0.8 - I_B R_B = 4.2 - 1.2$

$\Rightarrow V_{IL} = 3V$

Also, at some point, Q_P starts operating in OFF since V_{EB} voltage becomes less than 0.7V.

$\therefore V_{OH} = 4.8V \quad V_{IH} = 4.3V \quad V_{IL} = 3V \quad V_{OL} = 0V$

b. Let's first consider OH case.



Q_p' is OFF since $V_{EB_{Q_p'}} = 0.2V < V_{EB(on)}$

$\Rightarrow$ no current flows through Q_p'.

$$I_C = \frac{4.8}{R_C}$$

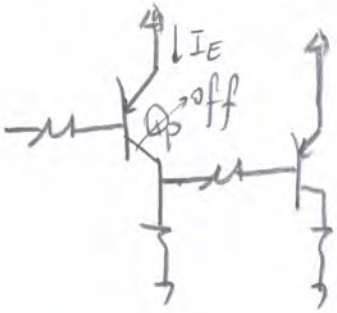
$$I_B = \frac{4.2}{R_B}$$

$$I_E = I_C + I_B$$

$I_E = 2.82mA$

$P_{OH} = I_E V_{DD} = 14.1mW$

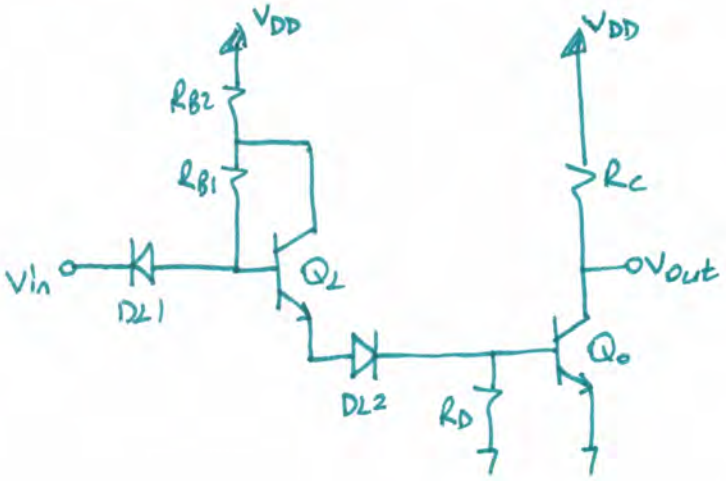
Let's consider OL case:



$I_E = 0 \Rightarrow P_{OL} = 0W$

$$\therefore P = \frac{P_{OH} + P_{OL}}{2} = 7.05mW$$

Q.2. For the modified DTL Family,

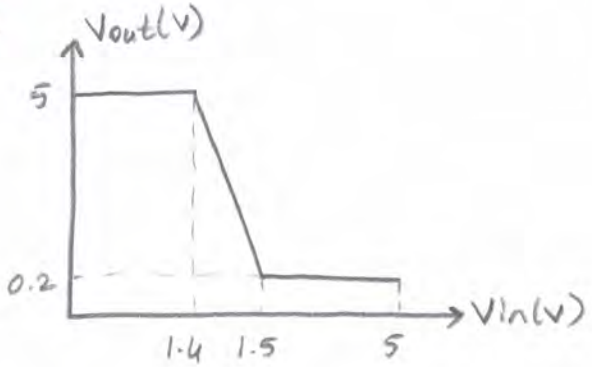


$\beta_F = 17$
$\beta_R = 0.8$
$V_{BE(F.A.)} = V_{BE(R.A.)} = 0.7V$
$V_{D(ON)} = 0.7V$
$V_{BE(SAT)} = 0.8V$
$V_{CE(SAT)} = 0.2V$
$\sigma_o = 0.6$
$R_{B1} = 2k\Omega$
$R_{B2} = 3k\Omega$
$R_C = 10k\Omega$
$R_D = 40k\Omega$
$V_{DD} = 5V$

a. Sketch the voltage transfer characteristics (VTC), and determine the critical parameters. ($V_{OL}, V_{OH}, V_{IL}, V_{IH}$)

b. Calculate the maximum fanout.

a.



Input: $0 \to V_{IL} \Rightarrow V_{out} = 5V$ (Q_o off)

At $V_{IL} \Rightarrow Q_o$ opens $\Rightarrow$ $0.7 + 0.7 = 1.4V$.

$V_{IL} = 1.4V$.

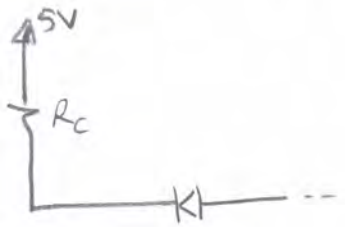
At $V_{IH} \Rightarrow Q_o$ saturates $\Rightarrow V_{IH} = 1.5V$.

$V_{OL} = 0.2V$
(Q_o in SAT)

Q_1 is always in F.A.R.

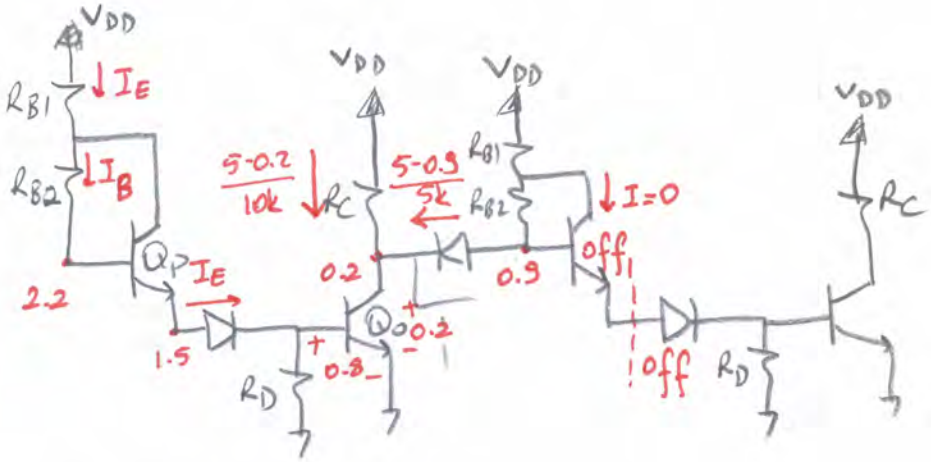
$\therefore V_{OH} = 5V,\ V_{IH} = 1.5V,\ V_{OL} = 0.2V,\ V_{IL} = 1.4V$

b. First, consider OH case.



Since no current can drawn by the gate, $N \to \infty$.

Now, consider OL case.



$$I_E R_{B1} + I_B R_{B2} = 5 - 2.2$$

$$((\beta_F + 1)2k + 3k) I_B = 2.8$$

$$I_B = 0.05mA \Rightarrow I_E = 0.9mA$$

$$I_{R_D} = \frac{0.8}{R_D} = 0.02mA \Rightarrow \underline{I_{BQ_0} = 0.88mA}$$

$$I_{EQ_0} = \left(\frac{5-0.9}{5k}\right) N + \frac{5-0.2}{10k}$$

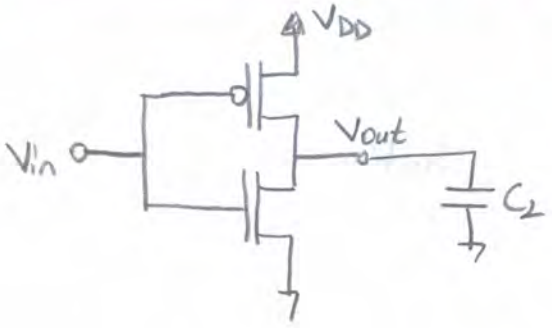
$$I_{EQ_0} \leq \sigma_0 \beta_F I_{BQ_0}$$

$$\frac{4.1}{5k} N + \frac{0.48}{k} \leq \frac{6}{10} \cdot 17 \cdot \frac{0.88}{k} \Rightarrow \frac{4.1}{5} N \leq 8.496$$

$$N \leq 10.36$$

$\therefore N = 10$ (We directly take N_{OL} as N since $N_{OH} \to \infty$)

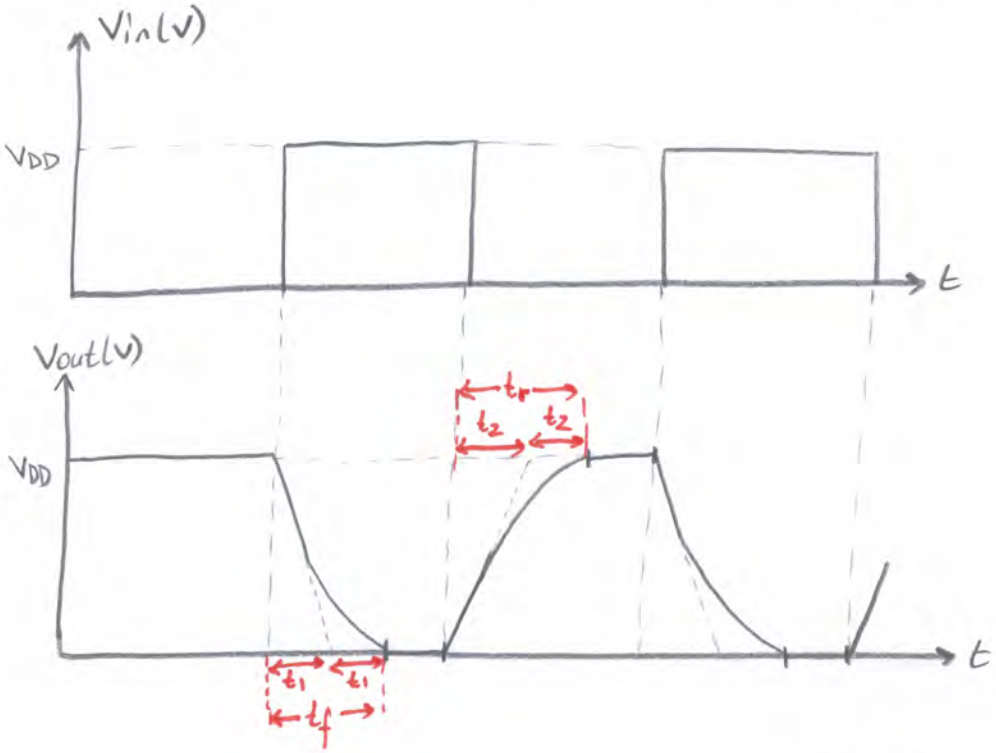
CMOS Charging a Capacitor



C_L : lumped capacitance of connected fanout.

$I_{OH} = I_{OL} = 0 \Rightarrow P_{OH} = P_{OL} = 0 \Rightarrow$ So, static power dissipation of CMOS is 0. $P_{static} = 0W$.

However; this is not the case for dynamic behavior.



* At the point where Vin becomes H, NMOS becomes operating in SAT. (It was off for OH case, initially). Then, at some point, it starts operating in linear mode till Vout = 0V. Time required for this transition is called fall time, denoted by t_f.

$$I_{DN} = -I_C = -C_2 \frac{dV_{out}}{dt}$$

$$dt = -C_2 \frac{dV_{out}}{I_{DN}(V_{out})} \quad , \; I_{DN} \text{ is a function of } V_{out}.$$

$$\Delta t = t_2 - t_1 = \int_{t_1(V_{out}=V_1)}^{t_2(V_{out}=V_2)} dt = -C_2 \int_{V_1}^{V_2} \frac{dV_{out}}{I_{D,N}(V_{out})}$$

Since Q_n changes its operation region, the above integral must be divided into two:

$$\Delta t = -C_2 \int_{V_1}^{V_{DD}-V_{TN}} \frac{dV_{out}}{I_{DN(SAT)}} - C_2 \int_{V_{DD}-V_{TN}}^{V_2} \frac{dV_{out}}{I_{DN(linear)}}$$

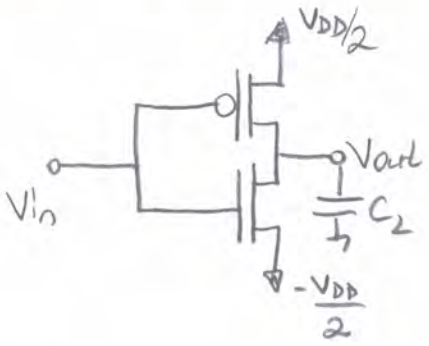
We know I_D for both SAT and linear regions, so we can put the corresponding expressions and values to find Δt which gives t_f for $V_1 = 0$, $V_2 = V_{DD}$.

★ Same procedure can be applied for rising characteristics and at that case, we should consider PMOS transistor. From corresponding derivations, rise time (t_r) can be calculated as above.

★ The most important fact about the dynamic behavior may be the maximum frequency that CMOS operates.

$$f_{max} = \frac{1}{T_{min}} \quad , \; T_{min} = t_f + t_r \Rightarrow \boxed{f_{max} = \frac{1}{t_f + t_r}}$$

★ Now, consider one of the most important problems in integrated circuits: heat problem. As transistors operate, they heat up. This is the case for CMOS, too. Now consider the following CMOS:



In this case, power dissipation will be the same with the previous case. However, in that case, only during rise time, a current drawn and this heats up the circuit instantaneously. However, in our new case, we divide the current into two and we separate them in time. This helps us to prevent excessive heat and this gives us time to cool down the circuit. So, we'll get better thermal management while the power dissipation is the same.

★ Suppose that we have a CMOS circuit and output is in 25% duty cycle. We want that CMOS will give the same output but it is in 50% duty cycle. (We want the output not to be damaged.) How can you achieve this?

Duty Cycle: $\frac{t_f}{t_f+t_r} \times 100$, Initially $\frac{t_f}{t_f+t_r} = \frac{1}{4} \Rightarrow \begin{matrix} t_f = t \\ t_r = 3t \end{matrix}$

$t_f \approx \frac{1}{I_{DSN}}$, $t_r \approx \frac{1}{I_{SDP}}$ $\qquad t_f \approx \frac{1}{K_{no}}$, $t_r \approx \frac{1}{K_{po}}$

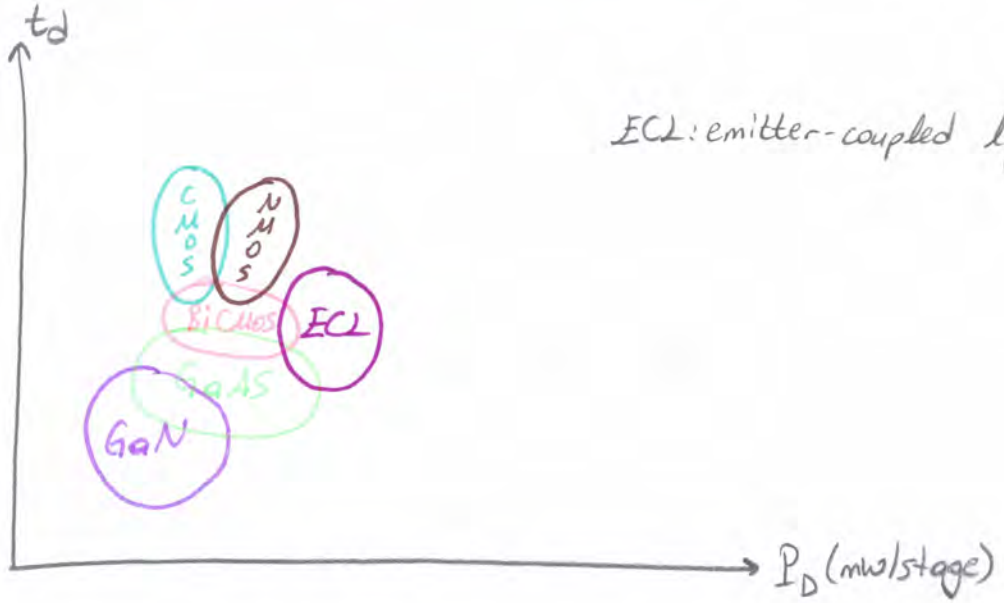
Initially $K_{no} = 3K_{po}$ ✓

If we take $t_f = t_r = 2t \Rightarrow K_{no}' = \frac{K_{no}}{2}$ ✓ ⇒ weaker NMOS

$K_{po}' = \frac{3K_{po}}{2}$ ✓ ⇒ stronger PMOS

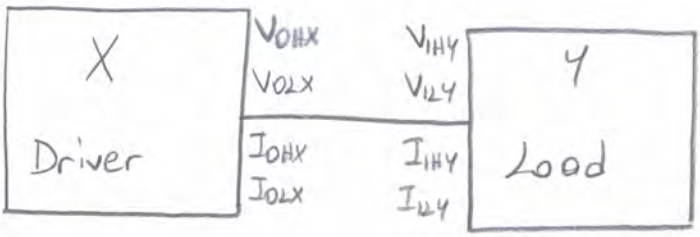
We should manipulate K_n and K_p values as above.

Interfacing Different Logic Families



We should choose the best one to manufacture our logic circuits. The best one seems to be GaN, but it is very expensive, so it is only used in very important designs. (Also, it is hard to produce.) After GaN, GaAs and BiCmos seems very logical, but they are also very expensive. ECL gives high performance, but P_D is too high, so we should not choose it.

Now, we are left with NMOS and CMOS. Their performances are approximately same, but CMOS is better for power dissipation. As a result, we choose CMOS in our circuits due to its cheap manufacturing process and low power dissipation.



1. Voltage capability

For X and Y be compatible, we need the following conditions:

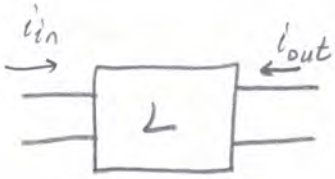
$$V_{OHX} \geq V_{IHY}$$
$$V_{OLX} \leq V_{ILY}$$

Also, if we are given noise margins, check the followings:

$$V_{OHX} - V_{IHY} \geq NMH$$
$$V_{ILY} - V_{OLX} \geq NML$$

2. Current capability

For this case, consider two port network as follows:



if $i_{OHX} \leq 10mA$, $i_{OHX(max)} = 10mA$ which makes the direction of the current inward and as a result, this will be sinking current

if $i_{OHX} = -10mA$, this makes the direction of the current outward, as a result, this will be sourcing current.

From that idea, we should first consider the current directions. if driver's and load's current directions are opposite, this driver cannot drive this load. However, if they are in the same direction, we should consider current magnitudes as in the following example.

Ex: We are given the following table.

	I_{OH}	I_{OL}	I_{IH}	I_{IL}
X	-10mA	-3mA	1.2mA	-0.7mA
Y	12mA	-2mA	2mA	0.8mA

(Suppose that voltage capabilities are satisfied.)

a. Can X drive Y? If so, find the maximum fanout.

OH: $\xrightarrow[X]{10mA}$ $\xrightarrow[Y]{2mA}$ ✓

OL: $\xrightarrow[X]{3mA}$ $\xrightarrow[Y]{0.8mA}$ ✓

So, X can drive Y.

$N_{OH} = \left\lfloor \frac{10}{2} \right\rfloor = 5$

$N_{OL} = \left\lfloor \frac{3}{0.8} \right\rfloor = 3$

$N = 3$

b. Can Y drive X? If so, find the maximum fanout.

OH: $\xleftarrow[Y]{12mA}$ $\xrightarrow[X]{1.2mA}$ ✗ Directions are not matched.

So, Y cannot drive X.

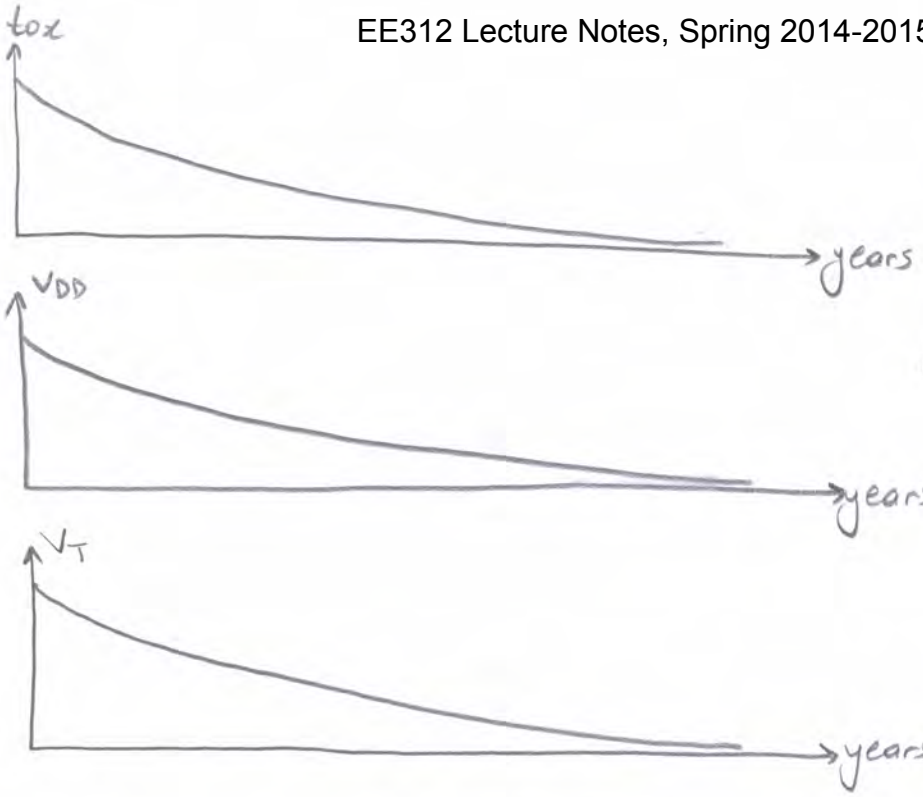
CMOS

Advantages

1. Zero static power dissipation. → Mobile applications.
2. Full rail-to-rail voltage swing ($0 - V_{DD}$)

	2007	2009	2011	2013	2015
L:	65nm	45nm	32nm	22nm	14nm ↓ 7 March 2015

By decreasing L the following graphs can be considered.



$(\leftrightarrow) E = \frac{V_G}{t_{ox}}$ ↓ ↓ (constant)

t_{ox}: thickness of the oxide at the gate of MOSFET.

V_G: gate potential.

* Low voltages result in lower power consumptions.

3. Smaller transition width.

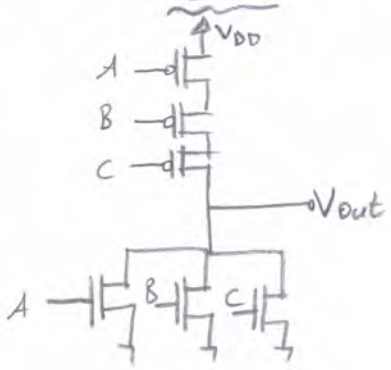
Disadvantages

CMOS has only one disadvantage to consider. This is the need for large number of transistors. More transistors mean more cost, so people try to find a way to reduce this number. For that purpose, Pseudo NMOS Logic was discovered, which reduces the number of transistors needed for design.

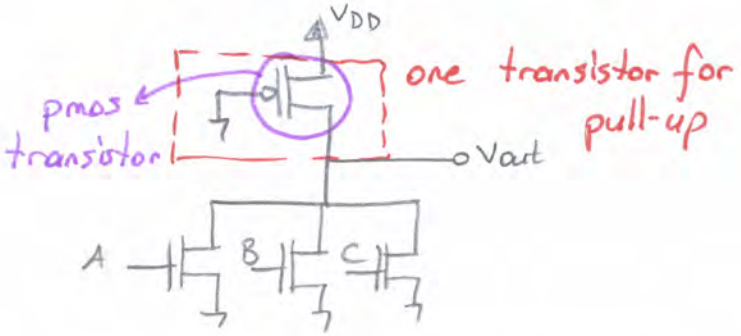
* Now, consider these two types on an example. Suppose that we are given a function as follows:

$$Y = A + B + C$$

CMOS



Pseudo NMOS



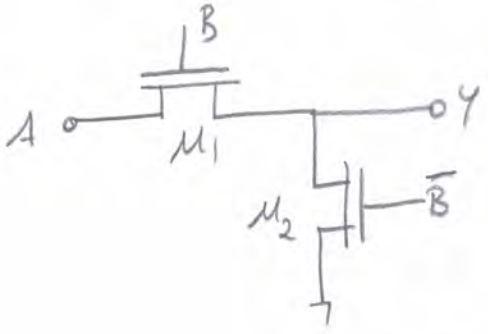
* It is clear that the number of transistors needed to implement this function by CMOS is 6, while it is only 4 for Pseudo NMOS. In general, maximum number of transistors needed is 2N (for N logic) for Pseudo NMOS and even in the worse case, their costs are equal.

Pass Transistor Logic

* The purpose of using pass transistor logic is to reduce the number of transistors used in the design compared to CMOS design.

* However, it is beneficial for only some special functions.

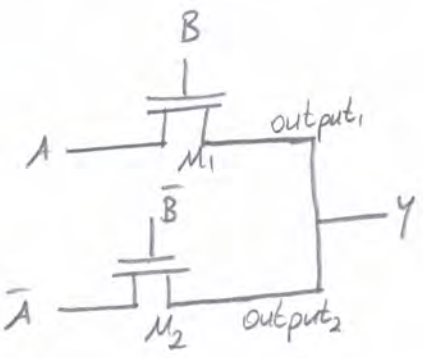
Ex: Implement $Y = AB$ by using pass transistor logic.



Let's obtain the truth table.

A	B	Y		M_1	M_2
0	0	0	→	off	on
0	1	0	→	on	off
1	0	0	→	off	on
1	1	1	→	on	off

Ex: Implement $Y = A\bar{B} + \bar{A}B$ using pass transistor logic.



By the design shown, it is achieved that one of the transistors will be on in a time. The off transistor gives floting output(High-Z) and the output is determined by the on transistor.

In any design, if two outputs are connected the following conditions should be considered. If they occurs, the design fails.

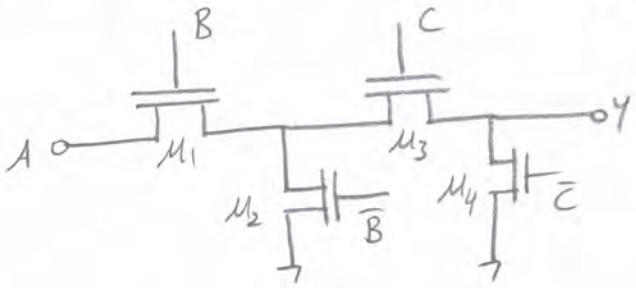
Output1	Output2
0	1
1	0
High-Z	High-Z

However, our design does not give such results. Let's find the truth table of our design.

A	B	output1	output2	Y	M1	M2
0	0	High-Z	1	1 →	off	on
0	1	0	High-Z	0 →	on	off
1	0	High-Z	0	0 →	off	on
1	1	1	High-Z	1 →	on	off

So, our design is valid and gives $Y = A\bar{B} + \bar{A}B$.

Ex: Implement $Y = ABC$ by using pass transistor logic



Let's check if this is a correct design.

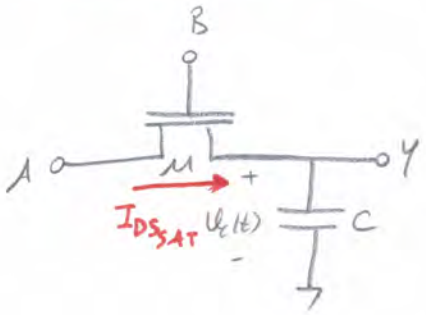
A	B	C	Y	M_1	M_2	M_3	M_4
0	0	0	0 →	off	on	off	on
0	0	1	0 →	off	on	on	off
0	1	0	0 →	on	off	off	on
0	1	1	0 →	on	off	on	off
1	0	0	0 →	off	on	off	on
1	0	1	0 →	off	on	on	off
1	1	0	0 →	on	off	off	on
1	1	1	1 →	on	off	on	off

Since the truth table is consistent with the function $Y = ABC$, our design is valid.

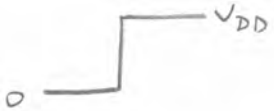
CMOS Transmission Gate

First, let's consider NMOS and PMOS cases seperately.

NMOS Case



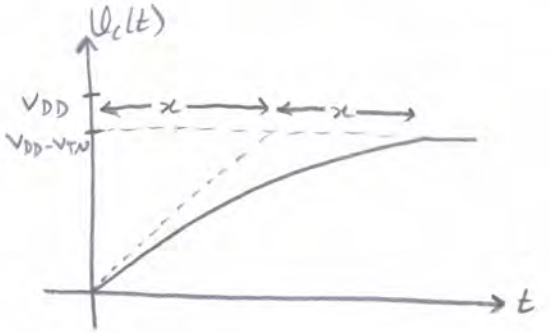
Assume capacitor is initially uncharged. Let $B = V_{DD}$ and A be in the following form.



At the transition moment, $V_{GS} = V_{DS}$. Since $V_{GS} - V_{TN} \leq V_{DS}$, M operates in SAT region. So, let's write the current expression:

$$I_{DS} = \frac{1}{2} K_n (V_{DD} - V_c(t) - V_{TN})^2$$

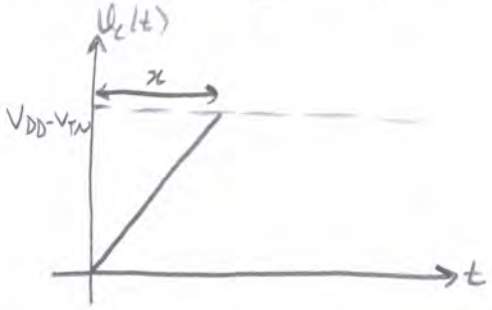
If we consider the current I_{DS} as in the equation above (real and most accurate case), we will obtain the following $v_c(t)$ vs t graph.



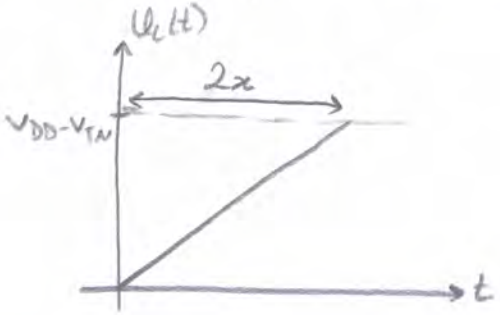
The intervals, stated by x, are equal by rule.

$v_c(t)$ cannot go above $V_{DD} - V_{TN}$ since in that case V_{GS} become smaller than V_{TN} and M become OFF. Also, for all t, since $V_{DS} = V_{GS}$, M is always in SAT.

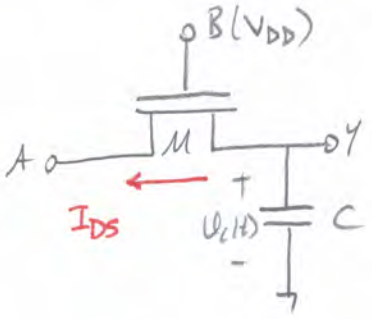
If we assume that I_{DS} current is constant and equal to its initial value (just for simplicity), we will obtain the following graph



If we assume that I_{DS} current is constant and it is the average of initial and final values of I_{DS}, then, we will obtain the following graph.



We initially assumed that the capacitor is uncharged and by the change of the state of A, it started charging. Now, consider discharging process. Even $v_c(t)=V_{DD}-V_{TN}$ is the maximum value for the previous case, let us assume that $v_c(t)=V_{DD}$ at the beginning of discharging.



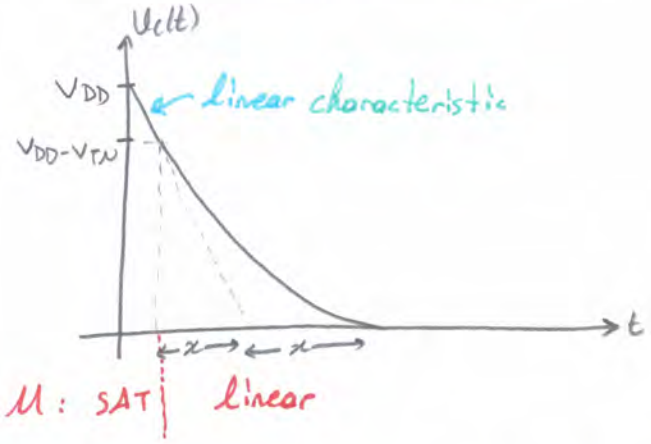
$v_c(t)=V_{DD}$ and the form of signal A is as follows:

Now, $V_{GS}=V_{DD}-0$, $V_{DS}=V_c(t)$. Initially, $V_{GS}-V_{TN}\leq V_{DS}$ and M is in SAT. However, after $V_{DS}=V_c(t)=V_{DD}-V_{TN}$, M becomes operating in linear region.

✱ During M is in SAT, $I_{DS(sat)} = \frac{K_n}{2}(V_{DD}-V_{TN})^2$ and it is constant. This results in a linear characteristics in $v_c(t)$ vs t curve. After $v_c(t)$ being $V_{DD}-V_{TN}$, I_{DS} has the following expression:

$$I_{DS(lin)} = K_n\left[(V_{DD}-V_{TN})v_c(t) - \frac{v_c^2(t)}{2}\right]$$

Now, let us plot $v_c(t)$ vs t graph.

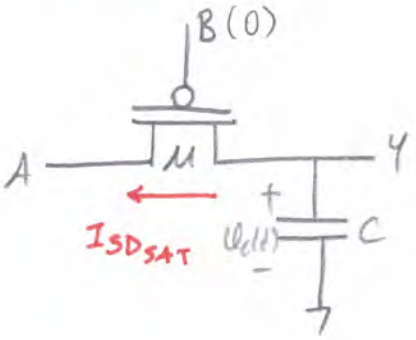


✱ Now, we are left with the question of what is the time required for the capacitor to discharge or charge? This time can be obtained by the following formula:

$$t = \frac{C\,\Delta V}{I_{DS}}$$

ΔV is the voltage difference between initial and final values of $v_c(t)$ and I_{DS} can be considered as the average value or initial value or the final value according to the statement of the question.

PMOS Case

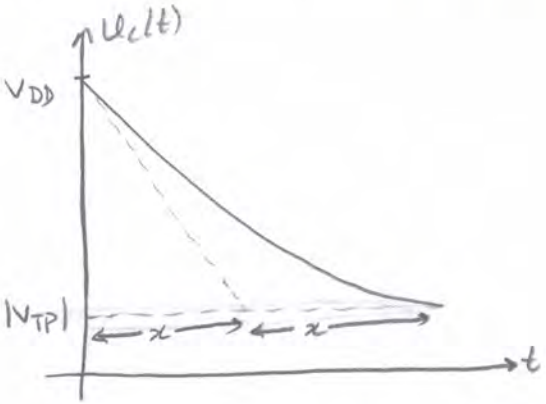


First consider the discharging behavior. Assume $v_c(t) = V_{DD}$ at the beginning and A has the following form:

$V_{SG} = v_c(t)$ and $V_{SD} = v_c(t)$. $V_{DS} - |V_{TP}| \leq V_{GS}$, so, M is in SAT region and during discharging its operation region does not change. For I_{SD}, we have the following expression:

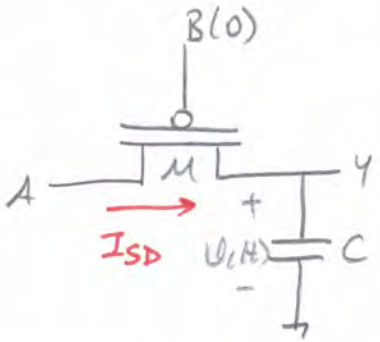
$$I_{SD} = \frac{1}{2} K_p (v_c(t) - |V_{TP}|)^2$$

This behavior continue till $v_c(t) = |V_{TP}|$ since beyond that point, M becomes OFF. So, we can obtain the following graph:



* It is observed that, the charging behavior of nmos resembles the discharging behavior of pmos. Also, as we will see, the discharging behavior of nmos resembles the charging behavior of nmos.

Now consider the charging behavior of this pmos circuit. Again, even $v_c(t)$ cannot fall to 0V, we, now, assume that at the beginning of charging process, $v_c(t)=0$.

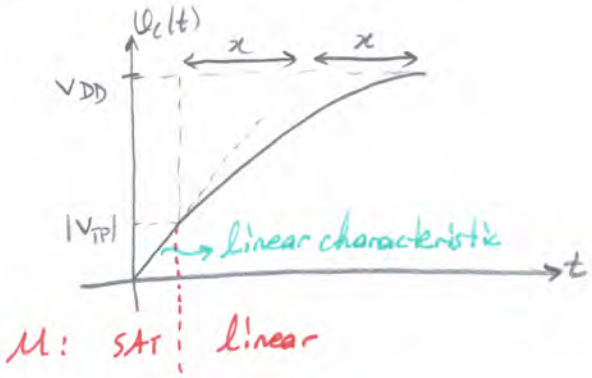


Assume A has the following form:

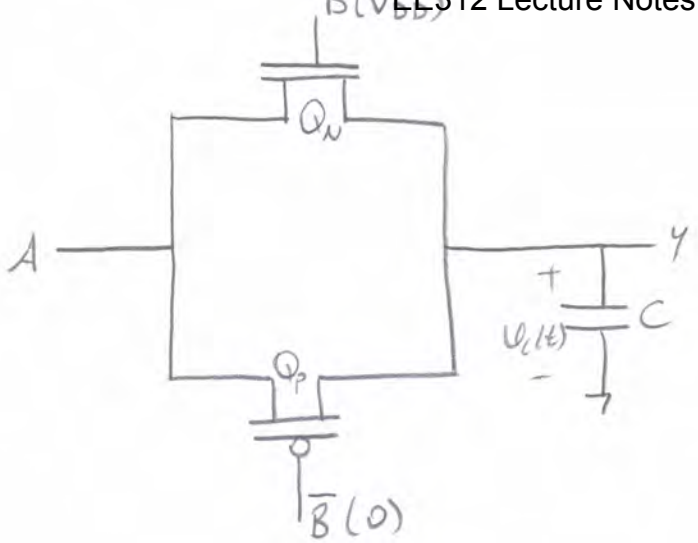
$V_{SG}=V_{DD}$

$V_{SD}=V_{DD}-v_c(t)$

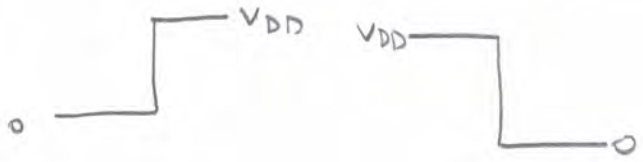
Initially, M is in SAT since $V_{GS}-V_{TP}>V_{DS}$. However, when $v_c(t)=|V_{TP}|$, M starts operating in triode region. As a result, we'll obtain the following $v_c(t)$ vs t graph.



After considering the characteristics of nmos and pmos gates in detail, we are ready to analyze the CMOS transmission gate very easily.



Assume that the capacitor is initially uncharged. Assume B is high and A has the following form



- Consider the first charge:

$V_{GS_N} = V_{DD} - V_c(t)$	$V_{SG_P} = V_{DD}$
$V_{DS_N} = V_{DD} - V_c(t)$	$V_{SD_P} = V_{DD} - V_c(t)$
$V_{GS_N} - V_{TN} \leq V_{DS_N}$	$V_{GS_P} - V_{TP} > V_{DS_P}$
So, Q_N is in SAT	So, Q_P is in SAT
till $V_c(t) = V_{DD} - \lvert V_{TN} \rvert$	till $V_c(t) = -V_{TP}$
since at that point	since at that point
Q_N becomes OFF	Q_P becomes operating in linear region.

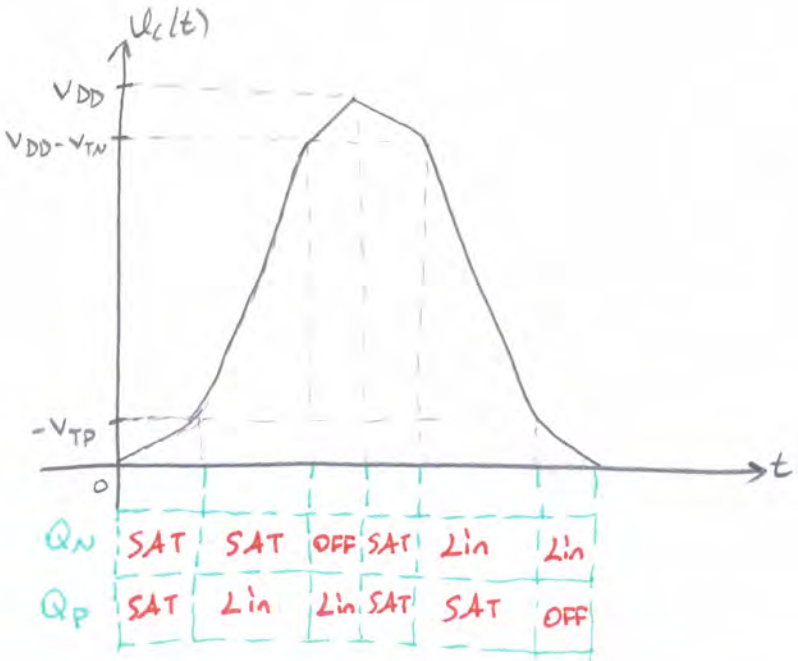
$V_c(t)$ will be V_{DD} at the end of charging period even Q_N is OFF. The reason is the existance of Q_P transistor.

- Now consider the second charge in A:

$V_{GS_N} = V_{DD}$	$V_{SG_P} = V_c(t)$
$V_{DS_N} = V_c(t)$	$V_{SD_P} = V_c(t)$
$V_{GS_N} - V_{TN} \leq V_{DS_N}$	$V_{GS_P} - V_{TP} > V_{DS_P}$
So, Q_N is in SAT till $V_c(t) = V_{DD} - V_{TN}$. After that point, Q_N is in triode region	So, Q_P is in SAT till $V_c(t) = -V_{TP}$. After that point Q_P will be off

$v_c(t)$ will be 0V at the end of discharging period even Q_P is OFF. The reason is the existance of Q_N.

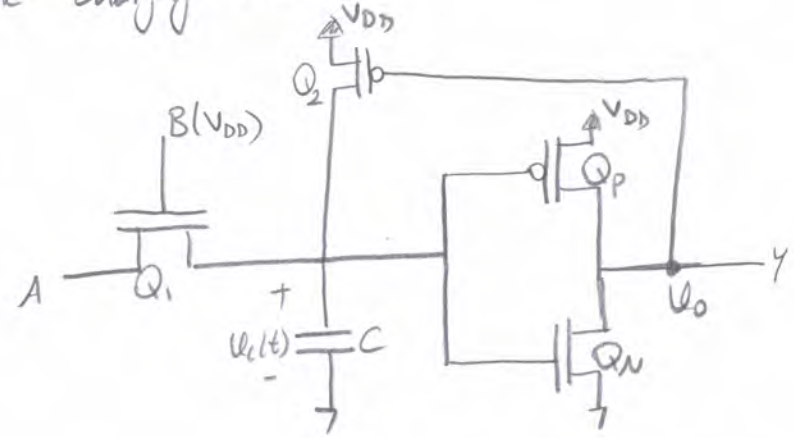
✯ Now let's draw the $v_c(t)$ vs t graph:



The shape of the curve is not consistent with the reality but it's just representative for important purposes.

✯ The advantage of using CMOS transmission gate is the ability to get 0V and V_{DD} without any loss due to V_{TN} and V_{TP}.

✯ Now consider the circuit given below which is designed to reduce the charging time.

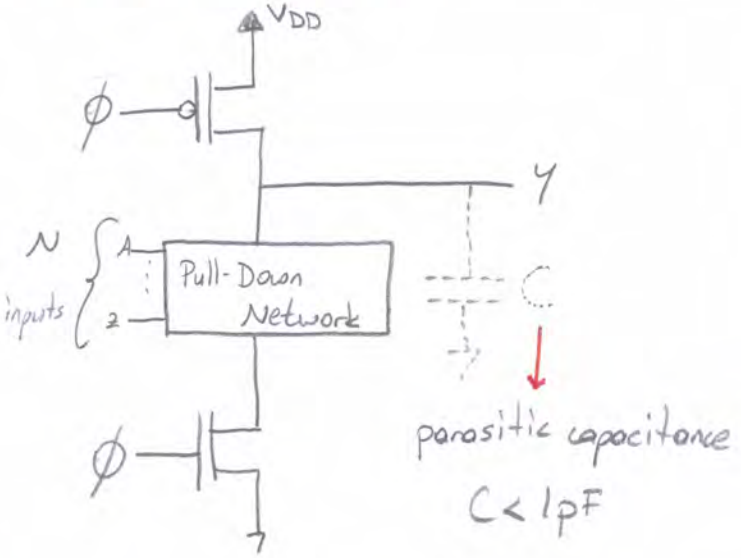


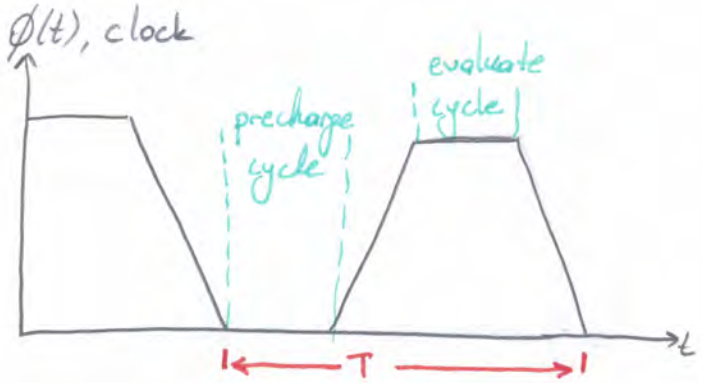
Assume that the capacitor is initially uncharged. So, Q_P is in linear region $\Rightarrow v_o = 5V$ $\Rightarrow Q_2$ is off. At the point where $v_o = V_{DD} - |V_{TP}|$, Q_2 becomes ON and it helps the capacitor to charge which results in a lower charging time. However, the disadvantage of this design is it increases the discharging time since the current of Q_2 will still try to charge the capacitor while the capacitor is trying to discharge.

Static Logic

This is the type of logic we have considered so far. In static logic, the number of transistors used is very high and due to this high cost, we have a motivation to reduce this number.

Dynamic Logic





★ The motivation to consider dynamic logic was reducing the number of transistors used in design. Let's see if this is the case.

CMOS ⟶ $2N$ transistors : static logic
Dynamic ⟶ $N+2$ transistors : dynamic logic
} $2N \geq N+2$

⇒ For $N > 2$, dynamic logic has less number of transistors, so it seems, we achieved our goal.

✱ However, dynamic logic has a disadvantage: output is available for only a fraction of time (evaluate cycle).

At the end of precharge, Y is high. Now consider evaluate cycle.

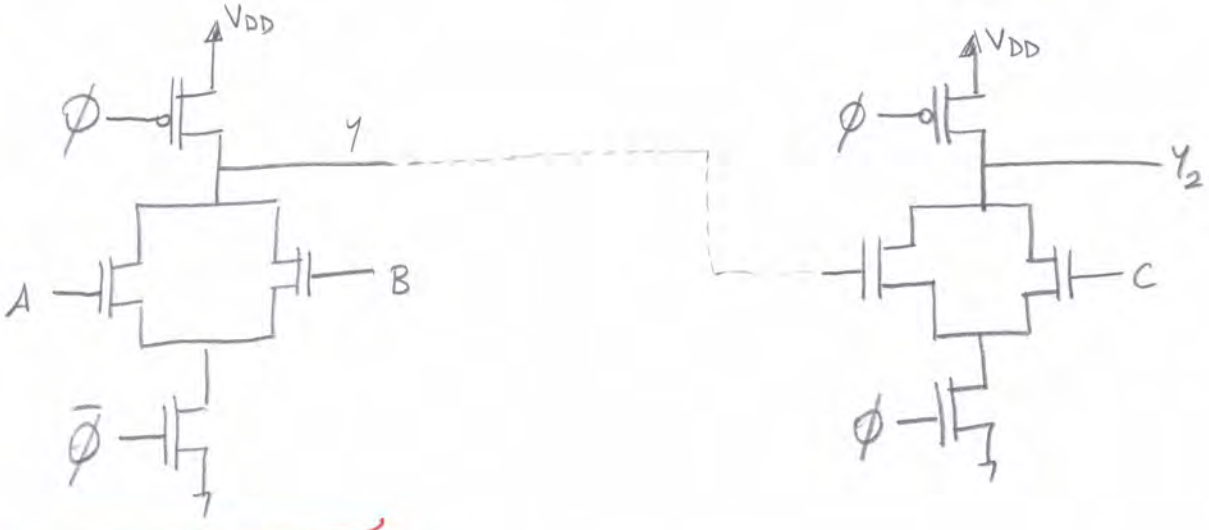
If the logic is false ⇒ no conduction ⇒ $Y=1$

If the logic is true ⇒ conduction ⇒ $Y=0$

✱ It is important to note that, input signal cannot change in the evaluate phase.

✱ Output can either stay the same or decrease, since there is no active pull up in the dynamic logic.

Ex: Let $Y=\overline{A+B}$. Implement this function by using dynamic logic.



Our desired design.

✱ Now assume that we are asked to implement $Y_2=\overline{Y+C}$. As a result, we tried our chance by the dashed connection. However, there is something wrong with this connection.

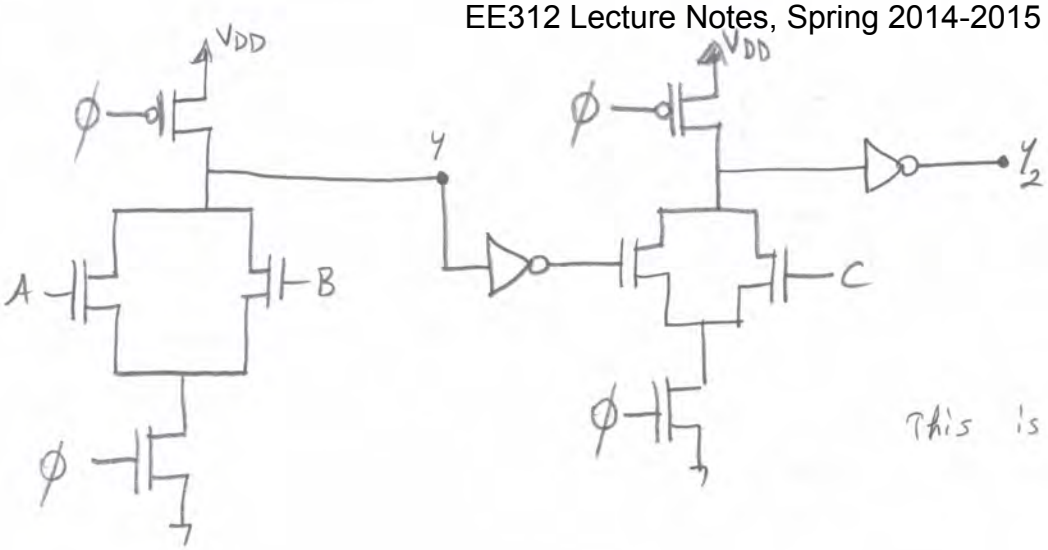
Let us find a counterexample to analyze the problem.

Let A=1 B=0
or
A=0 B=1
or
A=1 B=1
and
C=0

, At the end of precharge, $Y=1$, $Y_2=1$.

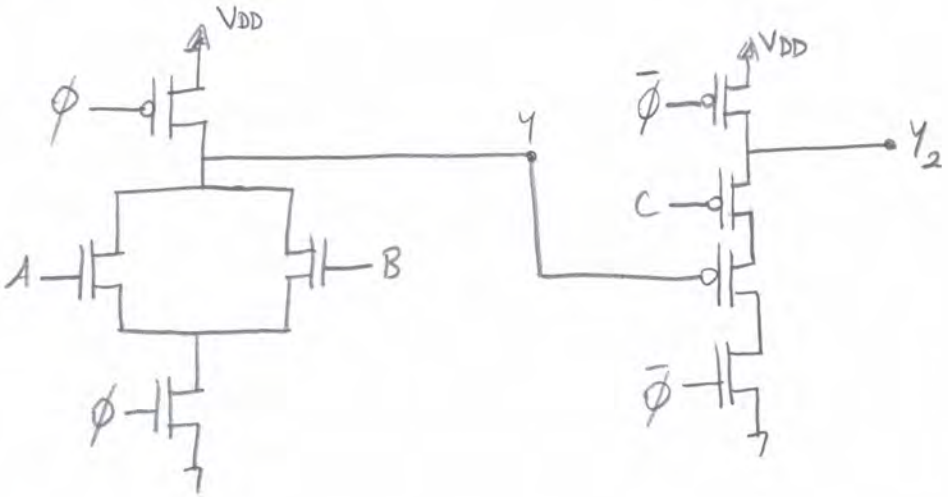
Just at the beginning of evaluate cycle, Y is 1 momentarily. However this causes the capacitor at Y_2 to discharge immediately and Y_2 becomes 0. After the change of Y from 1 to 0, the pull down network of second part is OFF. However, Y_2 is already 0 and due to the non-existance of an active pull-up network, Y_2 cannot be 1 and this causes problem in the implementation. This design gives wrong output Y_2 for the given case.

* So, it is clear that cascading dynamic circuits as in the figure in the previous page is not possible. So, what should we do? Cascading is necessary, obviously, so we should find a way to get rid of this issue.
* One way to achieve cascade connection between two dynamic logics is to consider an inverter at the output of each stage. The implementation is given in the following page.

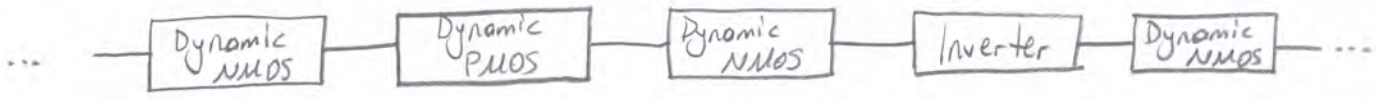


This is called domino logic.

* Another way is to use pmos dynamic logic after an nmos dynamic logic. The implementation is as follows:

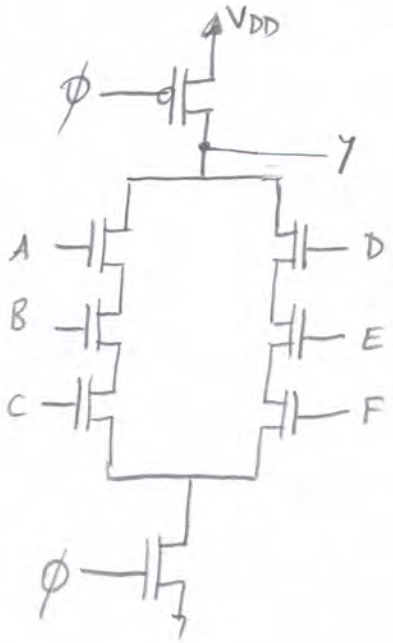


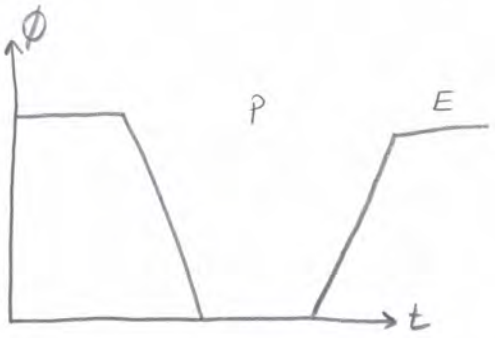
* For the last case it is important to note that always pmos is followed by nmos and vice versa. As an example, the following block diagram represents the possible connections.



Ex: Implement $Y = \overline{ABC + DEF}$ by

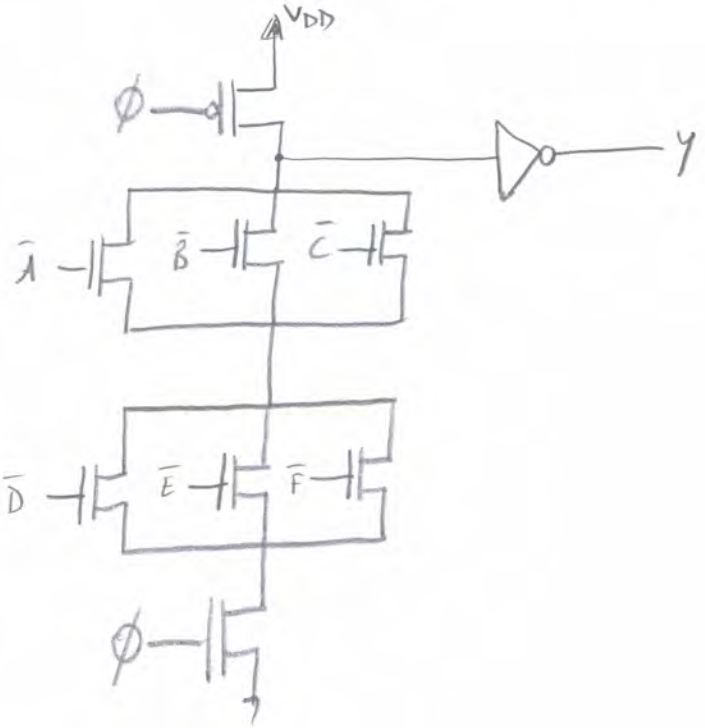
a. Using dynamic logic





b. Using domino logic

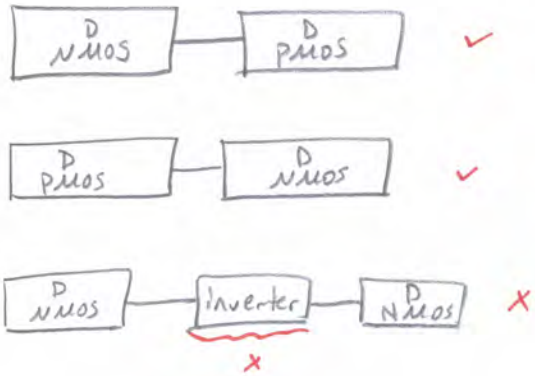
$$\overline{Y} = \overline{\overline{ABC + DEF}} = (\bar{A}+\bar{B}+\bar{C})(\bar{D}+\bar{E}+\bar{F})$$



Domino logic has only one static inverter.

c. Using dynamic logic, build a logic gate having at most 4 inputs.

No static logic allowed, pmos possible.

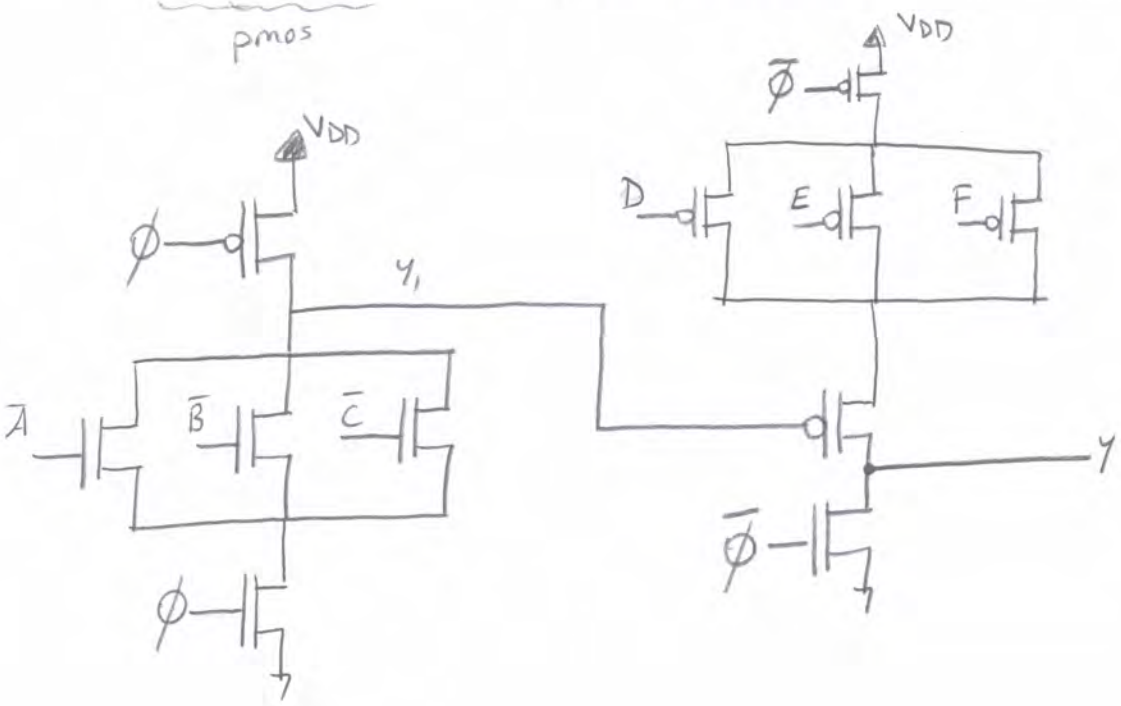


$Y = \overline{ABC + DEF}$, Let $Y_1 = ABC$, $Y_1 = \overline{\bar{A} + \bar{B} + \bar{C}}$

nmos

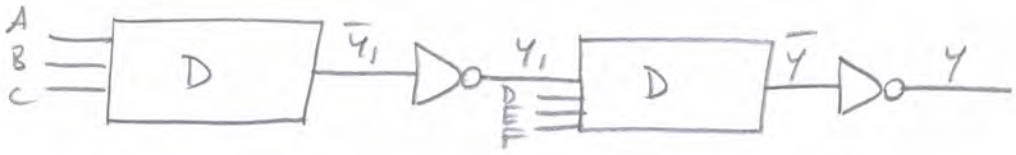
$Y = \overline{Y_1 + DEF}$ $\quad Y = \overline{Y_1}(\bar{D} + \bar{E} + \bar{F})$

pmos

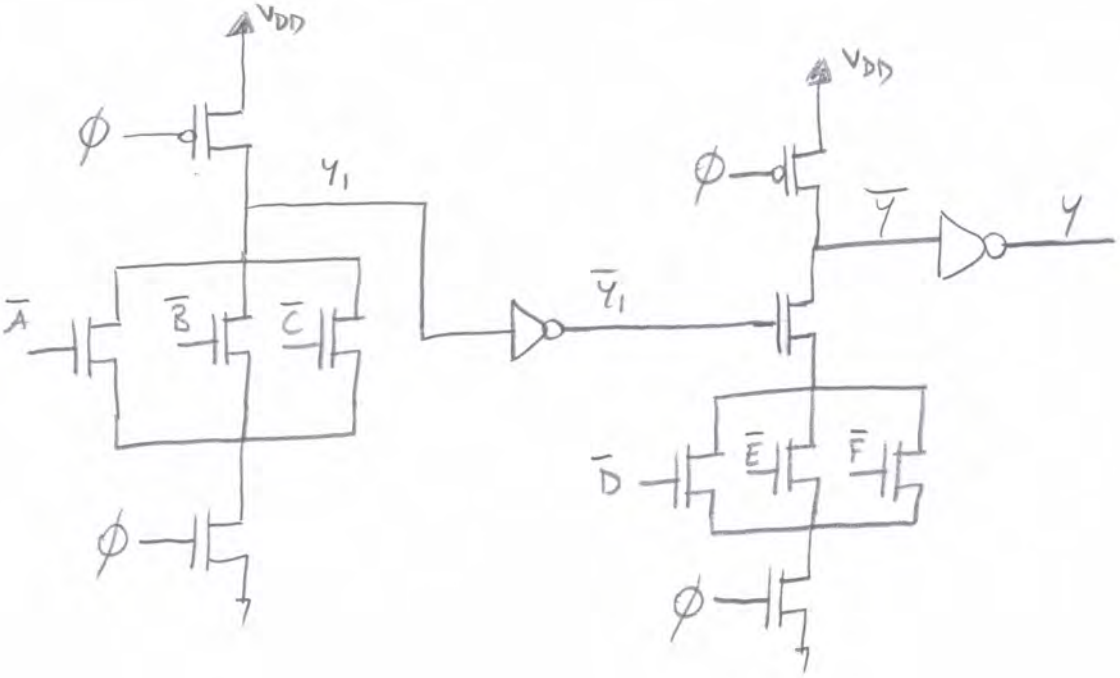


d. Using domino logic with a logic gate of most 4 inputs.

$Y_1 = ABC$, $\overline{Y_1} = \overline{ABC}$ at the end of first dynamic.



$\overline{Y} = Y_1 + DEF = \overline{\overline{Y_1}(\overline{D}+\overline{E}+\overline{F})}$

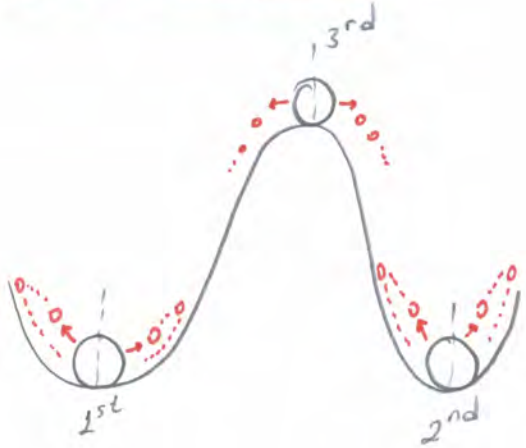


Dynamic Circuits

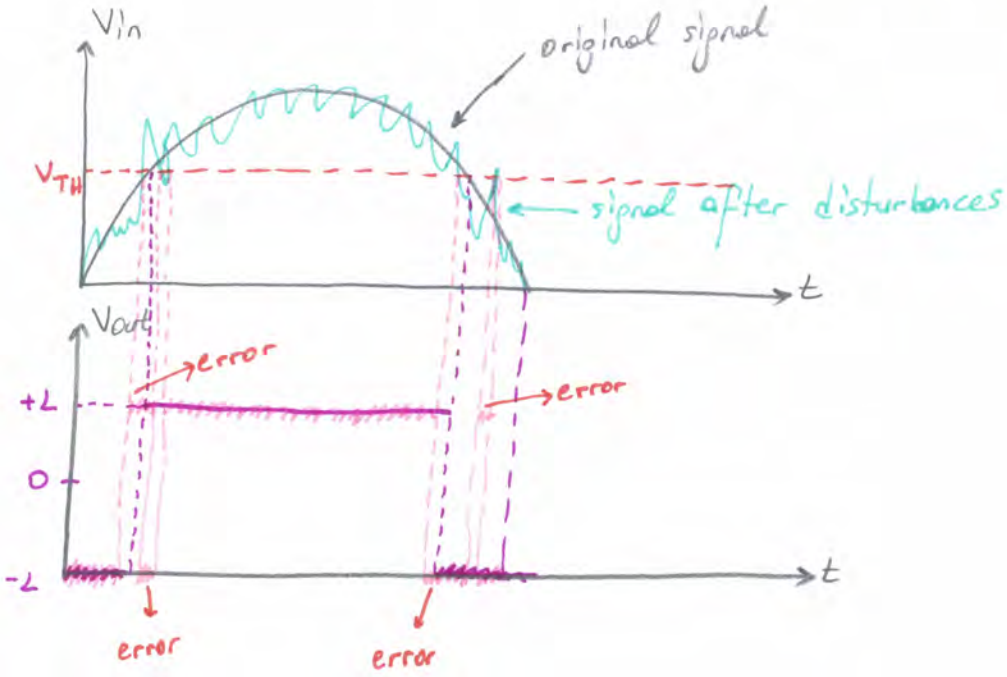
- They require less number of transistors.
- They are much faster than static logic
- As a result, we need to generate a clock signal.

Regenerative Circuits (Multivibrators)

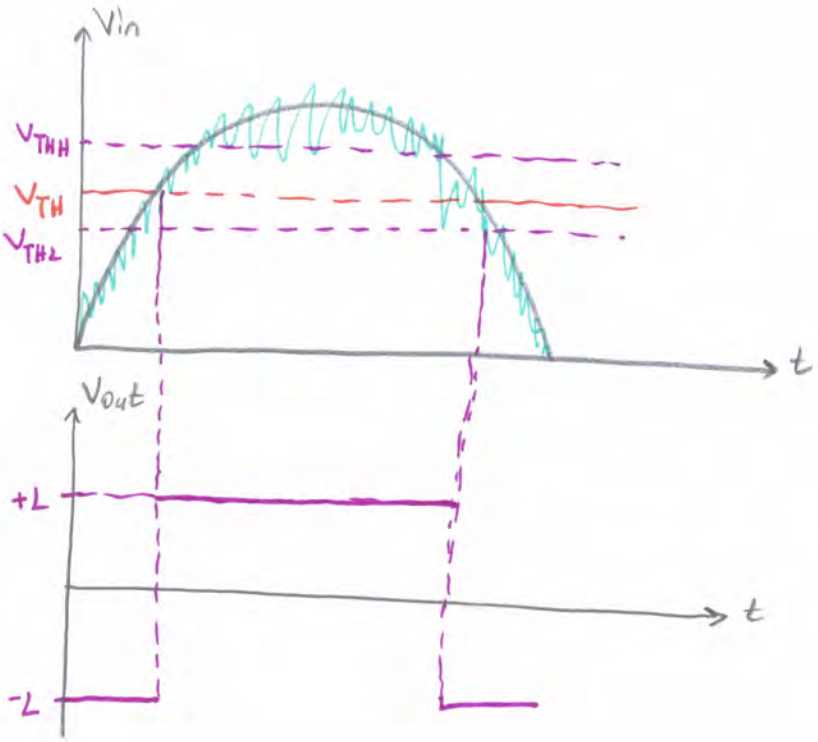
1. Bistable Multivibrator



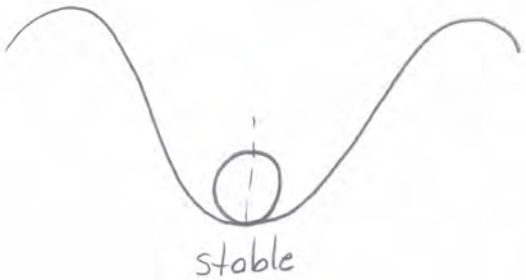
1st and 2nd states are stable since small disturbances (noise) do not affect a lot, in steady-state they come to their original position after some oscillations. However, 3rd state is unstable, clearly.



In order to avoid false errors, let us define V_{THH} and V_{THL} as follows:



2. Monostable Multivibrators



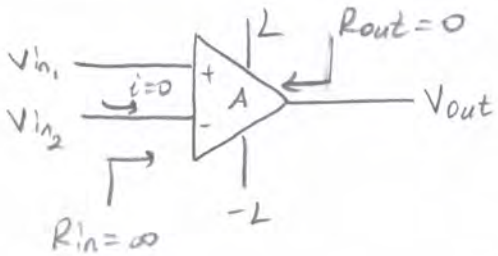
In this case, there is just a pulse.

3. Astable Multivibrators

These are clock generators.

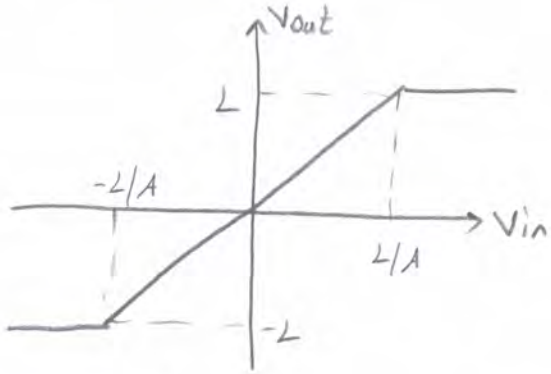
periodic signal running indefinitely.

Let us consider an opamp.



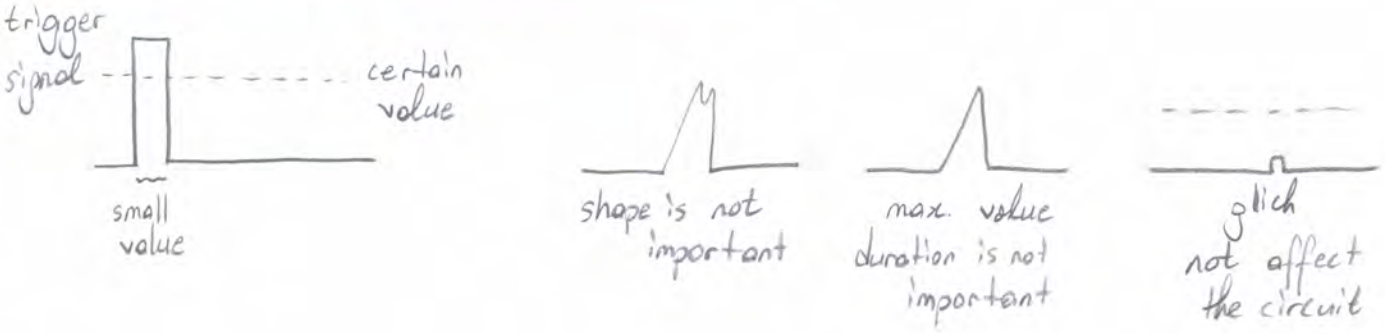
$e = V_{in_1} - V_{in_2}$

$A \approx 10^3 - 10^4$ v/v

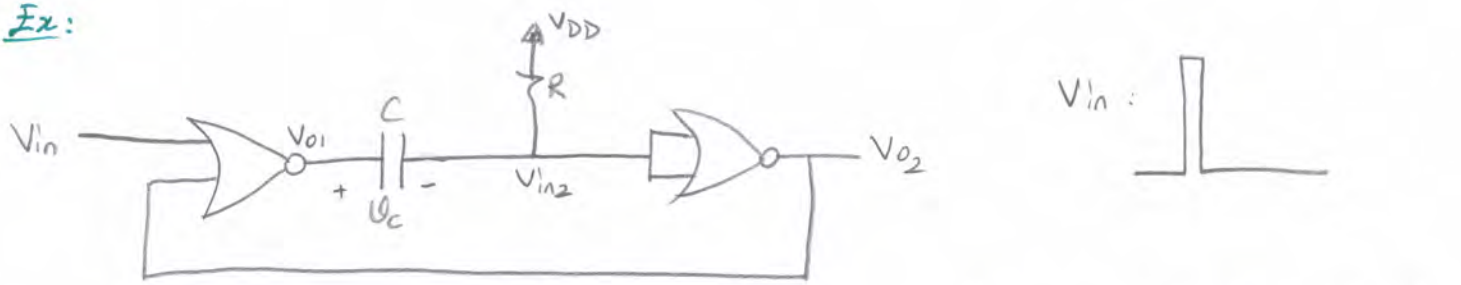


$$V_{out} = \begin{cases} +L & , \ e \geq L/A \\ Ae & , \ -L/A < e < L/A \\ -L & , \ e \leq -L/A \end{cases}$$

CMOS Monostable Multivibrator

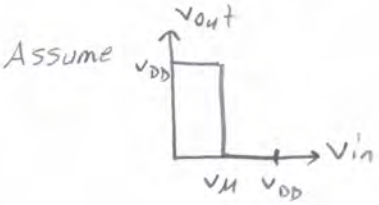


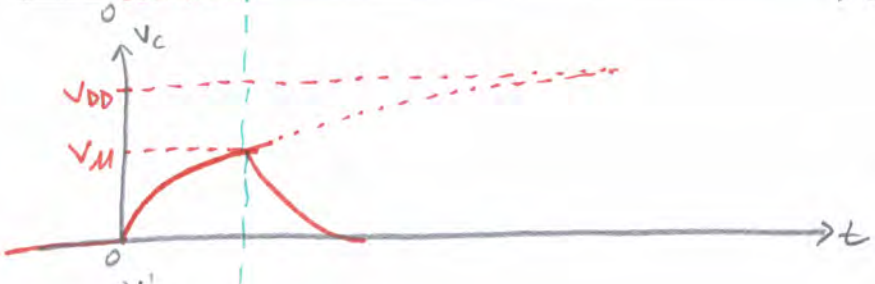
Ex:

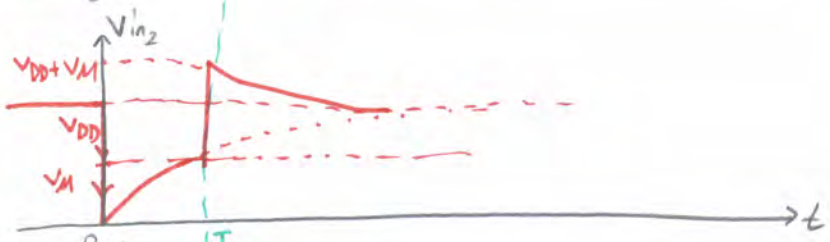


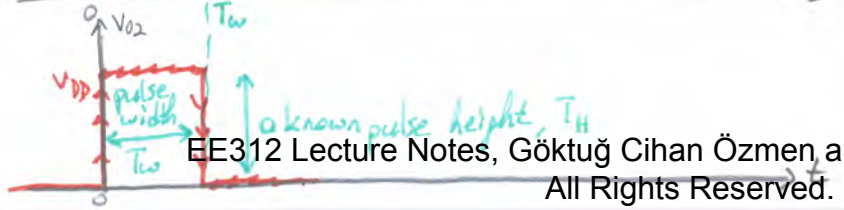
Initialization: Assume $V_{O_2} = 0 \Rightarrow$ since V_{in} initially zero $\Rightarrow V_{O1} = V_{DD} \Rightarrow V'_{in_2} = V_{DD}$

$V_{O_2} = 0$ ✓ Correct initialization.









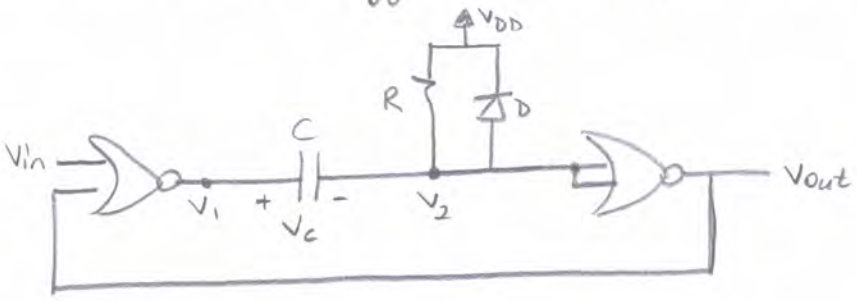
$$\tau = RC$$

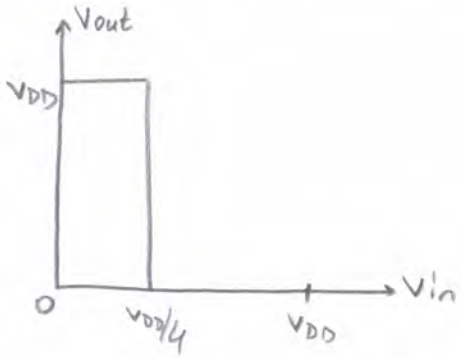
$$V_C(t) = V_{DD}(1 - e^{-t/\tau})$$

$$V_M = V_C(T_w)$$

$$\boxed{T_w = \tau \ln 2}$$

Ex: For the given CMOS gate illustrated in the figure, CMOS gate characteristics and tripper pulse waveform are given below:



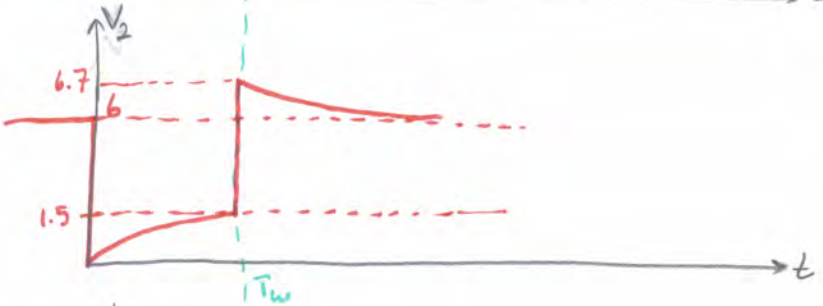


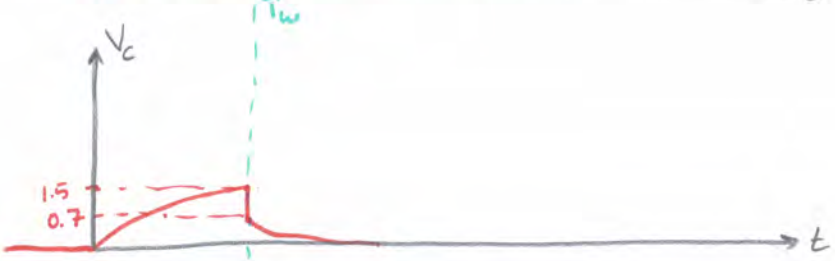
$C = 36pF$, $R = 12k\Omega$, $V_{D(on)} = 0.7V$, $V_{DD} = 6V$

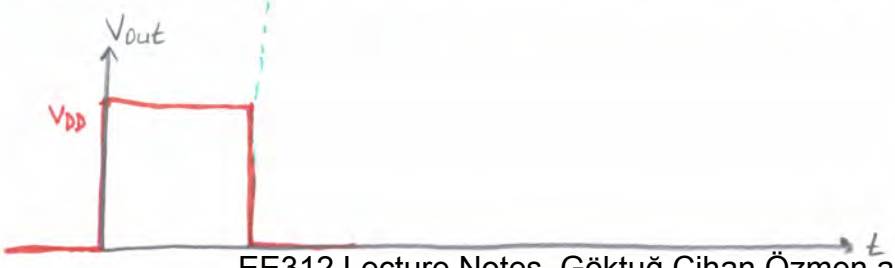
Assume that the capacitor is initially uncharged and a short trigger pulse is applied in the input V_{in} at $t=0$.

Initialization: $V_{out} = 0V$

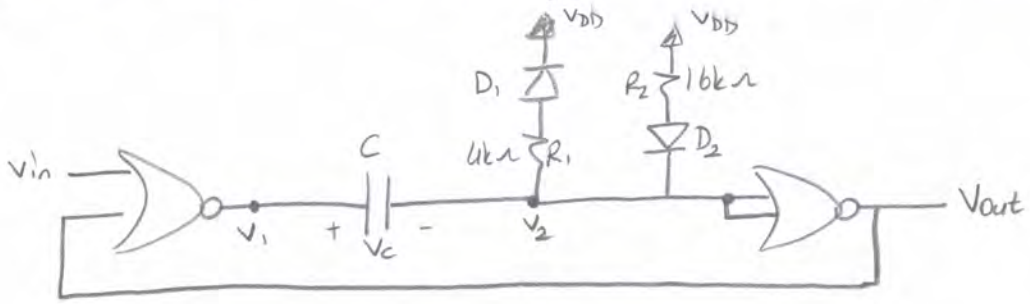
(verified in the previous example)

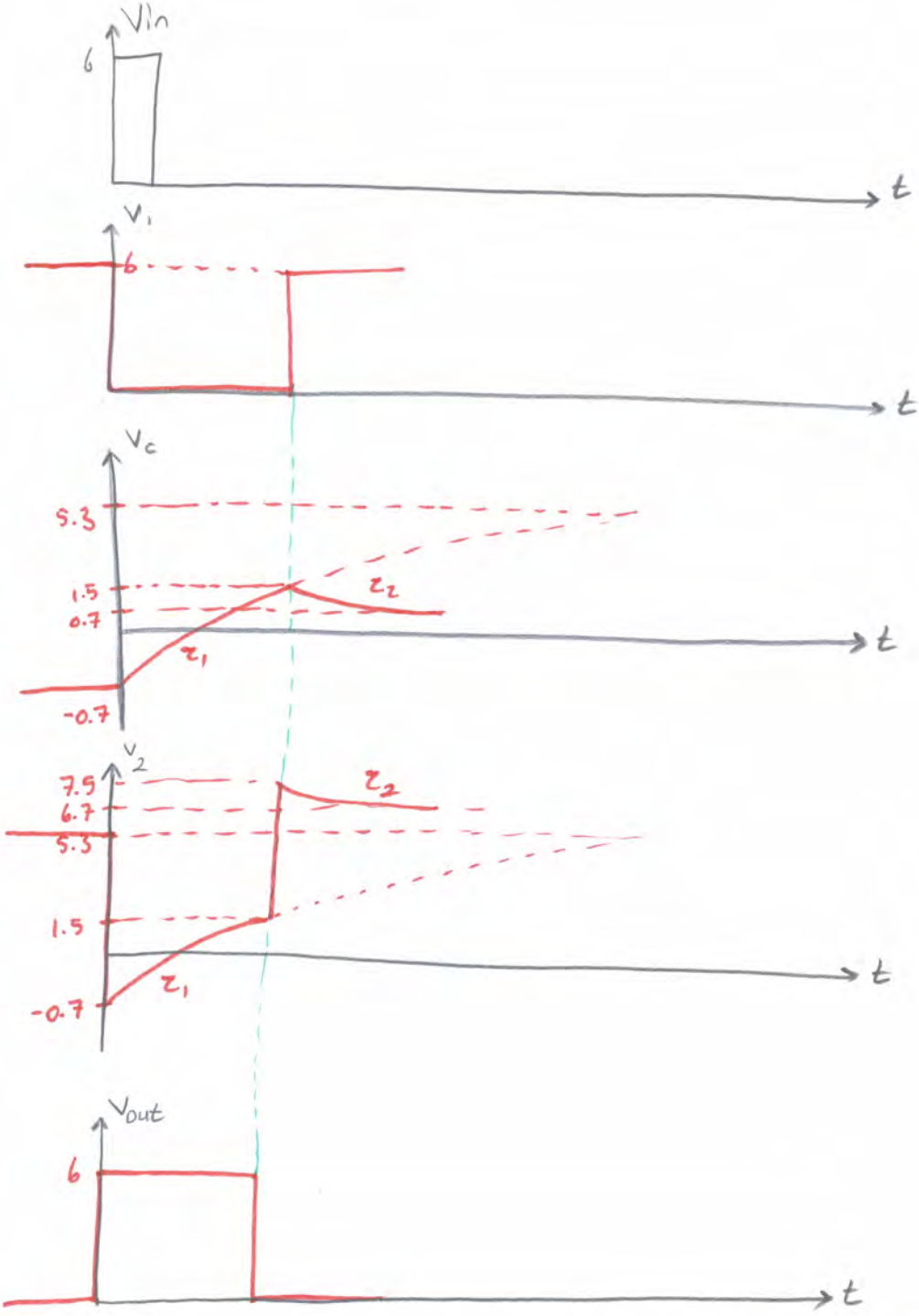






Ex: For the circuit given in the previous example, assume that with same charges we have the following circuit. (V_{TC} is the same for CMOS)



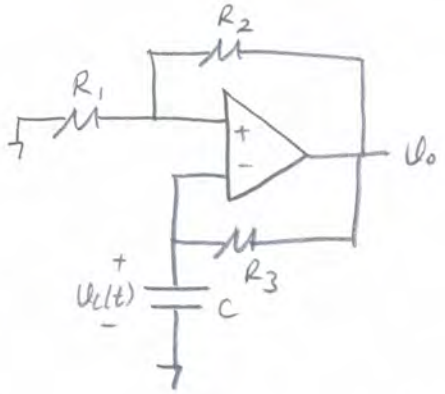


$\tau_1 = R_2 C$

$\tau_2 = R_1 C$

★ It is important to note that the positive and negative poles of V_c potential may change according to the conditions.

Generation of Square Waveforms using Astable Multivibrators



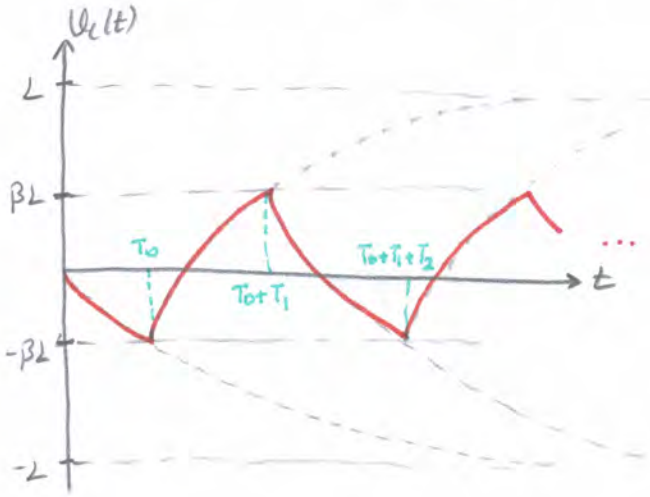
$v_c(0^-) = 0V$

Assume $v_o = -L$ initially.

$\Rightarrow V_+ = \frac{-LR_1}{R_1+R_2}$, $V_- = 0$

$V_+ < V_- \Rightarrow v_o = -L$ ✓

Let us define $\beta = \frac{R_1}{R_1+R_2}$. Now let's draw $v_c(t)$ vs t graph.



Initially, $v_c = 0V$. $v_o = -L$

$\Rightarrow v_c$ becomes $-\beta L$ with $\tau = R_3C$

$\Rightarrow$ At $v_c = -\beta L \Rightarrow V_- = -\beta L$

$\Rightarrow V_- = V_+ \Rightarrow$ beyond that point $v_o = +L$

τ is the same for all t. $\Rightarrow$ Let us find the period. $T = T_0+T_1+T_2-T_0$

$\Rightarrow T = T_1+T_2$, $f = \frac{1}{T}$.

$\Rightarrow$ Duty cycle of this wave is $\frac{T_1}{T_1+T_2}$.

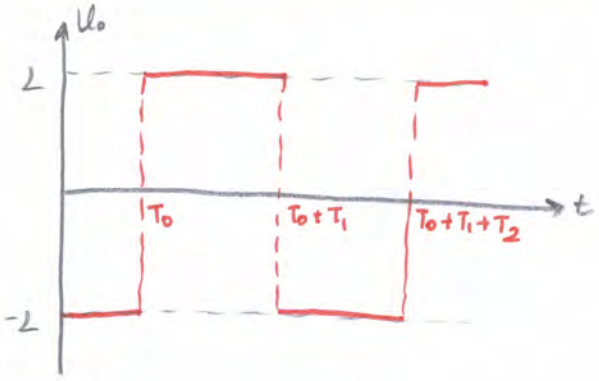
★ How can we find T_1 and T_2?

$v_c(t) = v_f + (v_i - v_f)e^{-t/\tau}$

$\Rightarrow$ for charging $v_c(t) = L + (-\beta L - L)e^{-t/\tau} \Rightarrow \beta L = L + (-\beta L - L)e^{-T_1/\tau} \Rightarrow$ find T_1.

$\Rightarrow$ for discharging $v_c(t) = -L + (\beta L + L)e^{-t/\tau} \Rightarrow -\beta L = -L + (\beta L + L)e^{-T_2/\tau} \Rightarrow$ find T_2.

* The shape of V_o signal is obvious but let us draw it.



* In our case, $T_1 = T_2 \Rightarrow$ which results in 50% duty cycle. Let us discuss what we can do to change f and the duty cycle.

The dependence of T_1 and T_2 on β is the same. So, changing β does not affect duty cycle. The dependence of them on τ is also the same. So, duty cycle is not affected by C and R_3 values, too. Also, L does not affect the duty cycle. There is one thing we can do. If the supply voltages are taken as follows, from $V_c(t)$ equations given in the previous page, the duty cycle changes.

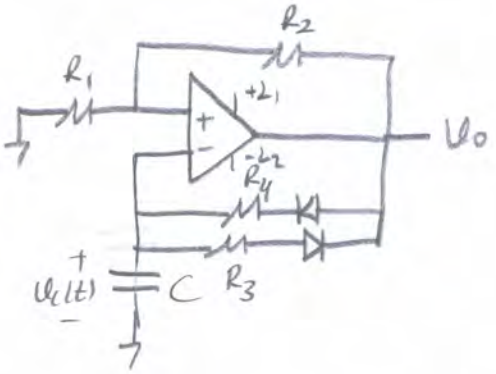
positive supply: $+L_1$
negative supply: $-L_2$
$\Big\} |L_1| \neq |L_2|$

Now we have another issue. What can we do to manipulate the frequency?

Well, it is obvious that the frequency directly depends on the τ value, so, we should change R_3 and C values such that τ changes.

Ex: Let us consider the following circuit with $V_{D(on)} = 0.7V$ and $|L_1| \neq |L_2|$.

$v_c(0^-) = 0$

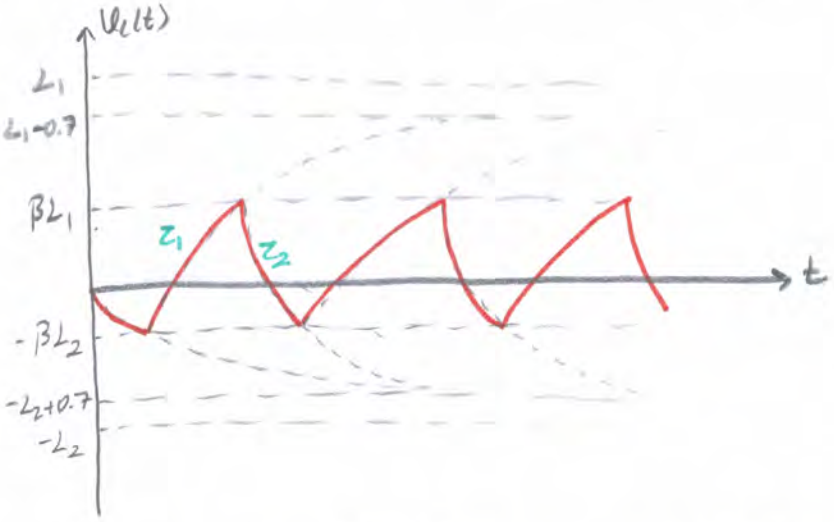


$v^+ = \beta v_o \left(\beta = \frac{R_1}{R_1+R_2}\right)$

Assume $v_o = -L_2$

$v^+ = -L_2\beta$, $v^- = 0$ $\Big\}$ $v^- > v^+ \Rightarrow v_o = -L_2$ ✓

Now, let us draw the $v_c(t)$ vs t graph.



$\tau_1 = R_4 C$

$\tau_2 = R_3 C$

For charging $v_i = -\beta L_2$, $v_f = L_1 - 0.7$ $\Big\}$ $v_c(t) = L_1 - 0.7 + (-\beta L_2 - L_1 + 0.7)\, e^{-t/\tau_1}$

$v_c(T_1) = \beta L_1 \Rightarrow$ find T_1.

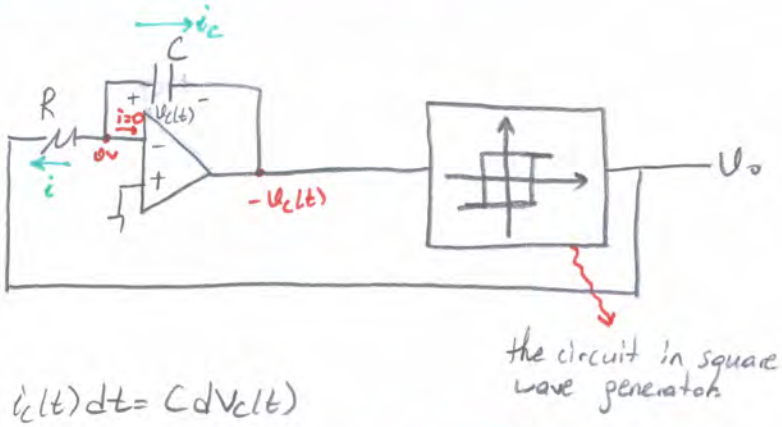
For discharging $v_i = \beta L_1$, $v_f = -L_2 + 0.7$ $\Big\}$ $v_c(t) = -L_2 + 0.7 + (\beta L_1 + L_2 - 0.7)\, e^{-t/\tau_2}$

$v_c(T_2) = -\beta L_2 \Rightarrow$ find T_2.

$\Rightarrow$ from T_1 and T_2 we can find duty cycle and f. It is clear that with the manipulations we made, now we have a different f and duty cycle from the initial case.

★ If we want to obtain a triangular wave from this circuit, we can decrease β and take the output from $v_c(t)$.

Triangular Wave Generation



the circuit in square wave generator

Assume $v_o = -L$

$\Rightarrow i = L/R$

$\Rightarrow i_c = -L/R$

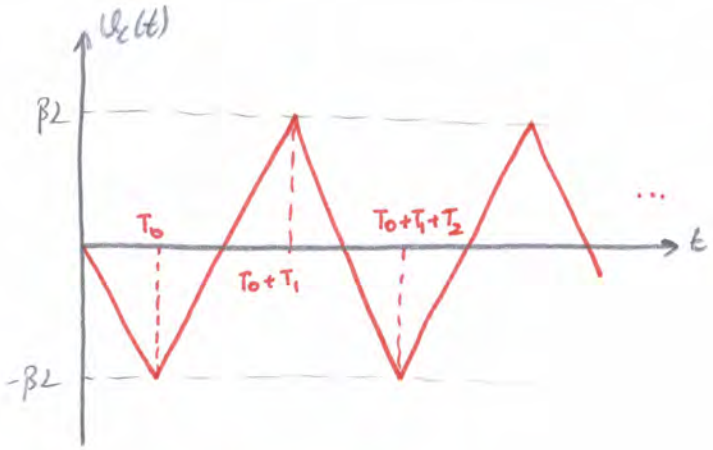
$$i_c(t) = C\frac{dv_c(t)}{dt}$$

$$i_c(t)\,dt = C\,dv_c(t)$$

$$\int \frac{-L}{R}\,dt = \int C\,dv_c(t) \Rightarrow \boxed{v_c(t) = \frac{-L}{RC}t}$$

$\Rightarrow$ At $v_c(t) = -\beta L \Rightarrow v_o = +L \Rightarrow v_c(t) = \frac{L}{RC}t$

Now, let us draw the $v_c(t)$ vs t graph.



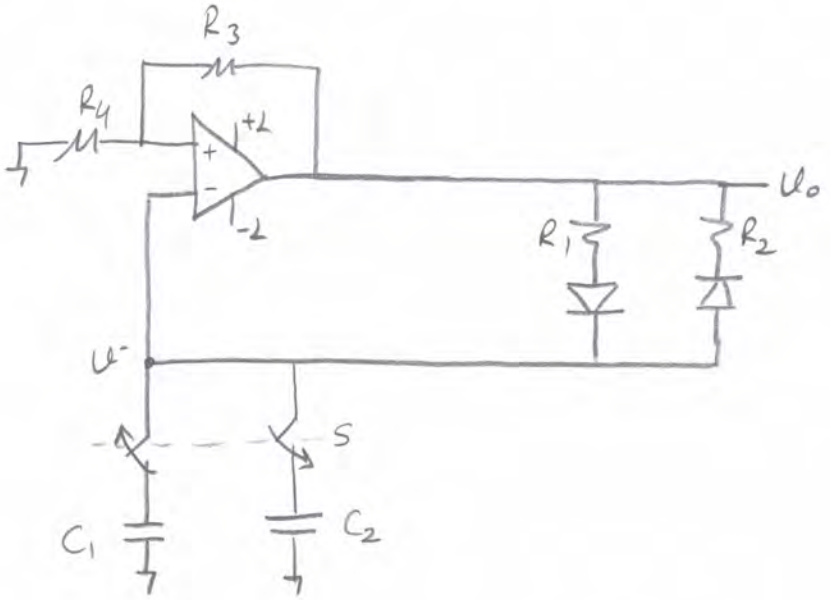
$$T_1 = \frac{2\beta L}{L/RC} = 2\beta RC$$

$$T_2 = \frac{2\beta L}{L/RC} = 2\beta RC$$

$$\boxed{T = T_1 + T_2 = 4\beta RC}$$

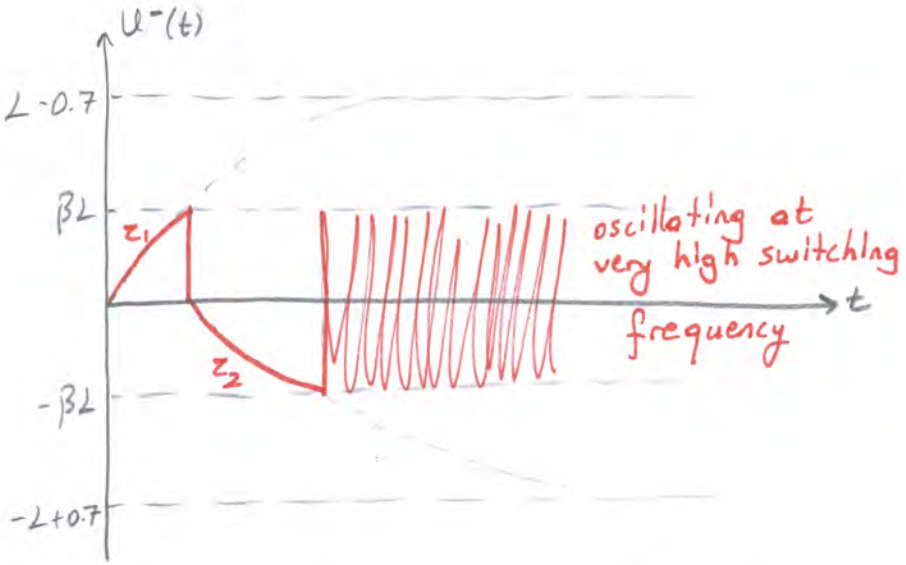
$$\boxed{\text{duty cycle} = \frac{T_1}{T_1+T_2} = 50\%}$$

Ex: A multivibrator circuit is given in the figure.



S switch is on (C_1) and off (C_2) when output is $+L$. S switch is off (C_1) and on (C_2) when output is $-L$. Assume that the capacitors are initially uncharged and $v_o = +L$. Draw $v^-(t)$.

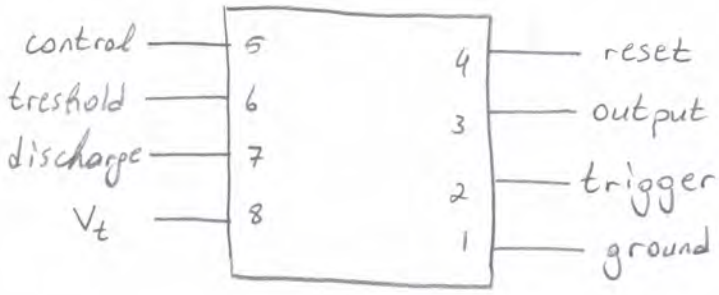
Let $\beta = \frac{R_4}{R_3+R_4}$, $\tau_1 = R_1C_1$, $\tau_2 = R_2C_2$



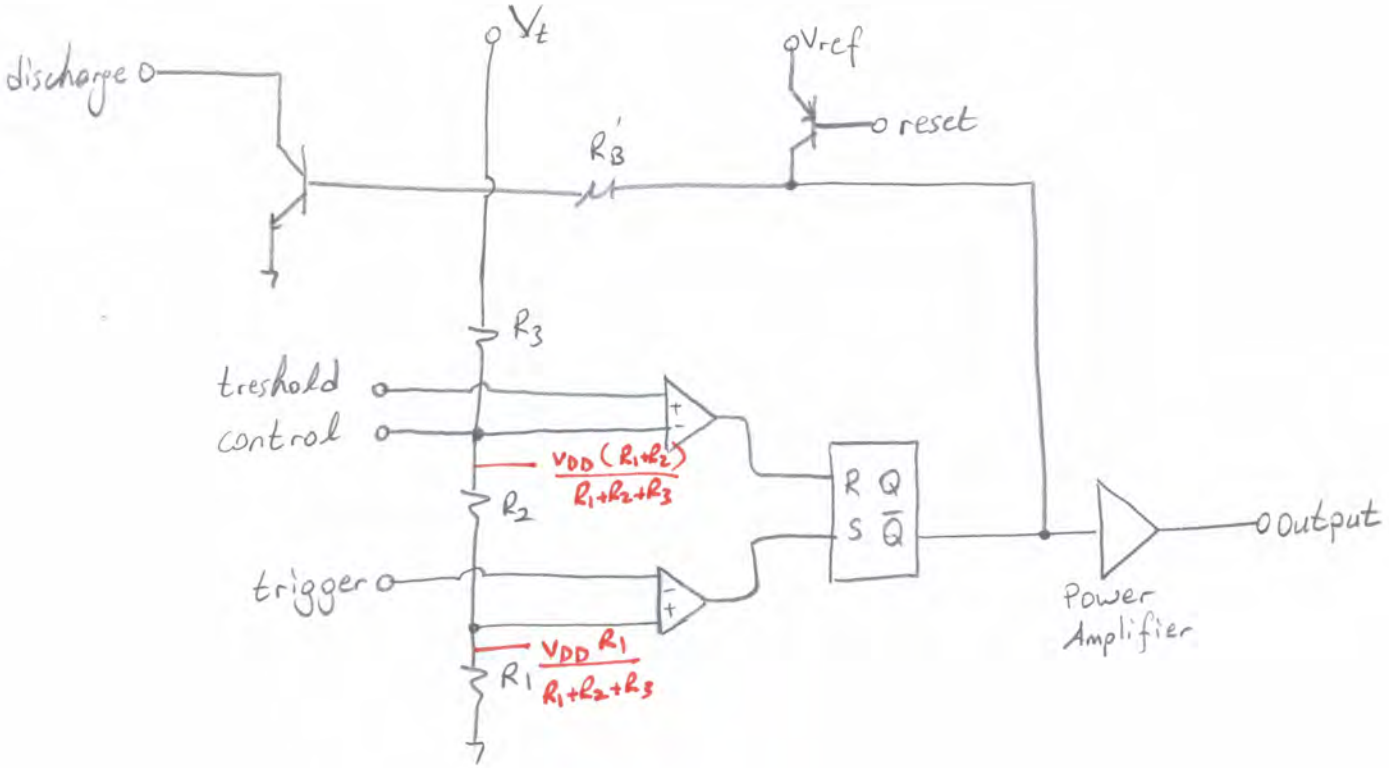
Initially $v^- = 0$. Till $v^- = \beta L$, $v_o = +L$. At that point $v_o = -L$ and switch is off for C_1 and on for C_2 which results in $v^- = 0V$. After that point, till $v^- = -\beta L$, we have τ_2 as in the figure.

However, after that point we have two caps with $v_1 = \beta L$, $v_2 = -\beta L$ which results in immediate changes in v_o voltage. As a result, $v^-(t)$ oscillates at a very high rate. (Only possible delay comes from switching.)

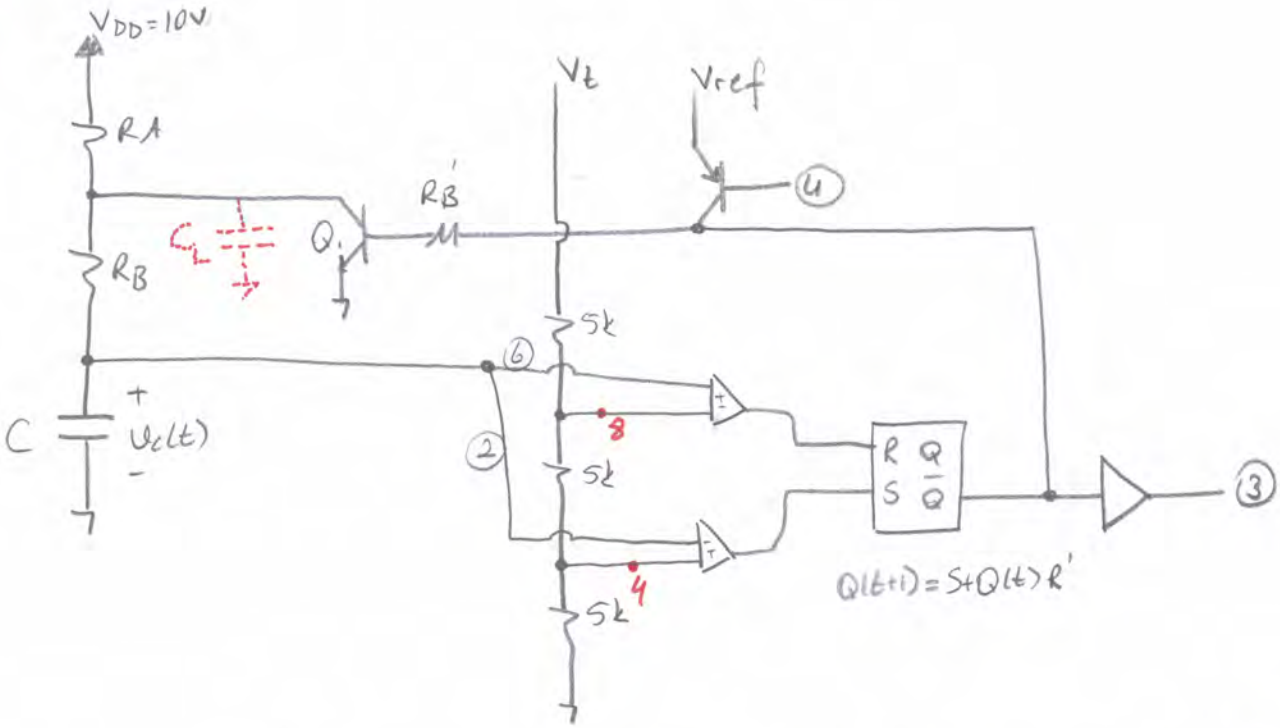
555 Integrated Circuit Timer



In our discussion, we will primarily be interested in trigger pin, treshold pin and discharge pin. The internal structure of this integrated circuit is as follows:



Ex:

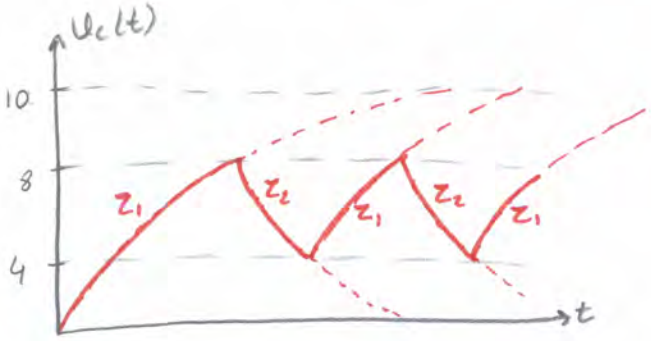


Assume $R_A = R_B$. Assume $v_c(0) = 0V$. Draw $v_c(t)$ vs t graph.

Initially, $v_c(t)$ starts charging with $\tau_1 = C(R_A + R_B)$. V_{CE} of Q_1 is very large so Q_1 is in F.A.

Initially, $R=0, S=1 \Rightarrow ③ = 1$. (Assume the circuit is initially reset.) At $v_c = 4V \Rightarrow R=0, S=0 \Rightarrow$ no change $\Rightarrow ③ = 1$.

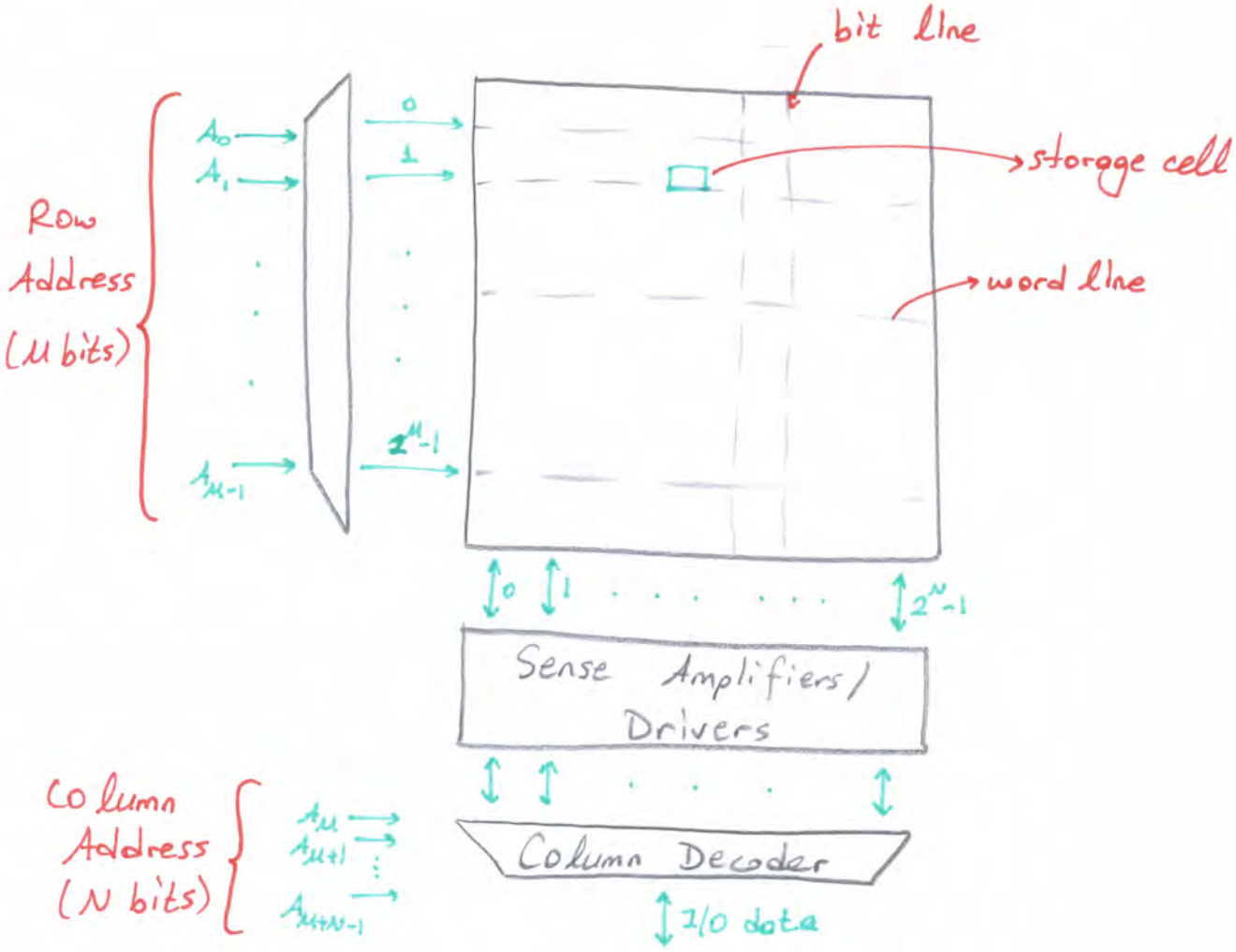
At $v_c = 8V \Rightarrow R=1, S=0 \Rightarrow ③ = 0 \Rightarrow Q_1$ is off $\Rightarrow$ C will be discharged through C_2 (too low) till $v_c = 4V$ since at that point $R=0, S=1$ $\Rightarrow ③ = 1 \Rightarrow$ C starts charging through $R_A + R_B$. This will continue indefinitely.



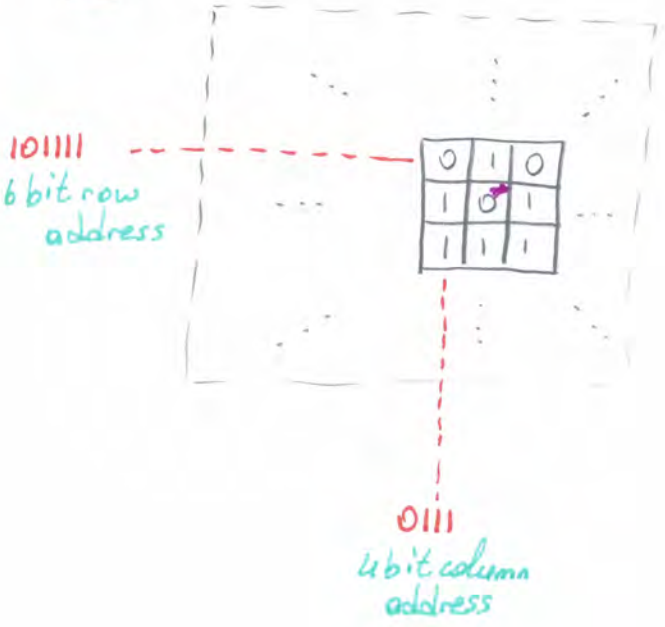
$\tau_1 = C(R_A + R_B)$

$\tau_2 = CR_B$

Semiconductor Memories



Ex:

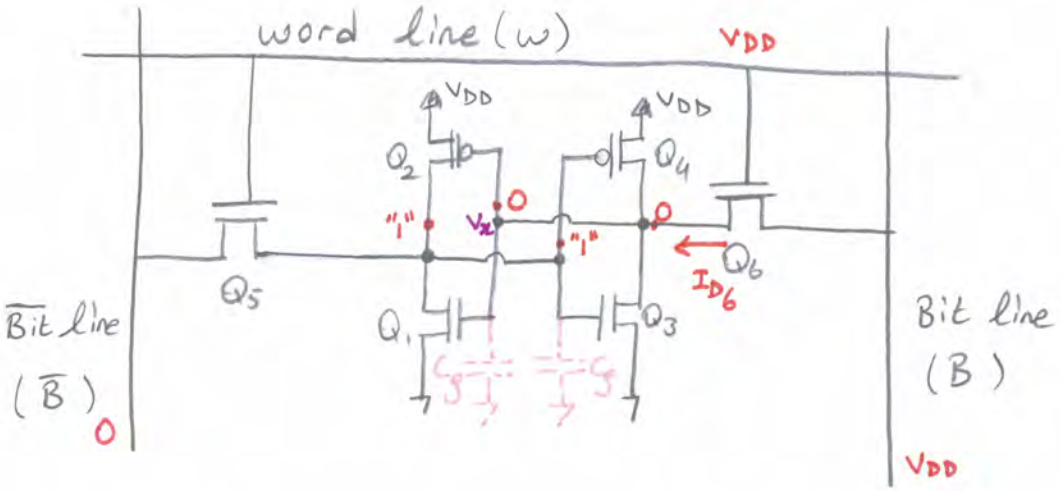


What is the address of *?

Row: 110000 (= 101111 + 000001)

Column: 1000 (= 0111 + 0001)

Static Memory Cell

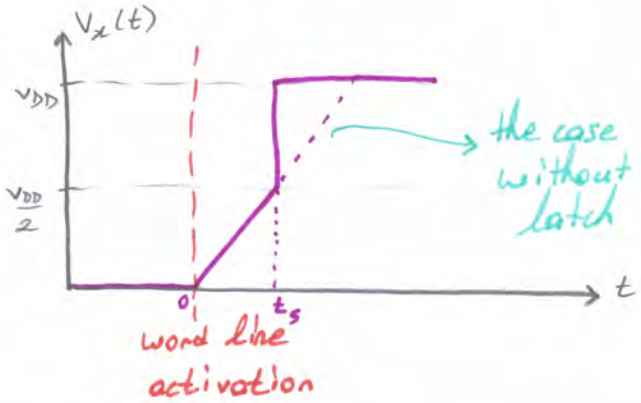


In this structure, we use 6 transistors for 1 bit information. It costs a lot, so it is not used nowadays.

★ Let us write "1".

Assume the following VTC for CMOS:

▨ : for this case



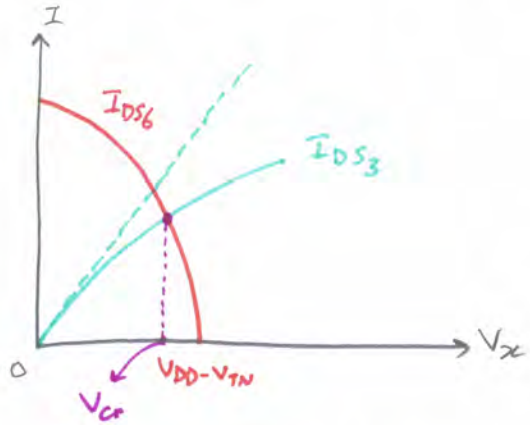
$$t_S = \frac{C_g\left(V_{DD} - \frac{V_{DD}}{2}\right)}{\frac{1}{2}k_{n6}\left(V_{DD} - V_{TN6}\right)^2}$$

time required for switching

★ Initially $V_x = 0 \Rightarrow$ [illegible]

$\bar{V}_x = V_{DD} \Rightarrow Q_3$ is on, Q_1 is off, Q_2 is on, Q_4 is off

We have I_{DS6} current from Q_6 and Q_3 transistor takes I_{DS3} current. As a result, we are left with $I_{DS6} - I_{DS3}$ current.



$$I_{DS3} = K_{n3}\left[(V_{DD}-V_{TN})V_x - \frac{V_x^2}{2}\right]$$

$$I_{DS6} = \frac{1}{2}K_{n6}(V_{DD}-V_x-V_{TN})^2$$

$$I_{net} = I_{DS6} - I_{DS3}$$

We have $V_{cr} \geq V_{DD}/2$, since if V_{cr} is greater than V_M, Q_4 would turn on to provide additional current.

$$\frac{1}{2}K_{n6}(V_{DD}-V_{cr}-V_{TN})^2 = K_{n3}\left((V_{DD}-V_{TN})V_{cr} - \frac{V_{cr}^2}{2}\right)$$

Let $V_{cr} = \frac{V_{DD}}{2}$, $V_{TN} = 1V$, $V_{DD} = 5V$

$$\frac{1}{2}K_{n6}(5-2.5-1)^2 = K_{n3}\left[(5-1)(2.5) - \frac{2.5^2}{2}\right]$$

$$1.125\,K_{n6} = 6.875\,K_{n3}$$

$$K_{n6} \gg 6.11\,K_{n3}$$

Let $K_{n6} = 7K_{n3} \Rightarrow K_{n6} = \frac{7W}{L}$, $K_{n3} = \frac{W}{L} \Rightarrow K_{n4} = \frac{5W}{2L}$

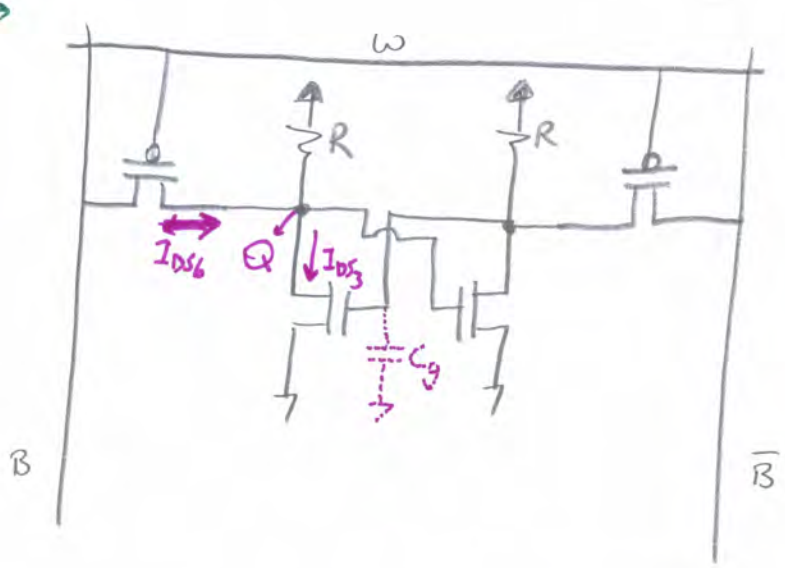
by the general property of cmos

$K_{n2} = \frac{5W}{L}$, $K_{n1} = \frac{W}{L}$

By the symmetry of the latch

★ We have observed CMOS latch, so far. The following latches are possible, as well.

→



Due to pmos transistors, B and $\bar{B}$ lines are changed.

$$t_{write} = \frac{C_g(V_{DD}/2 - 0)}{I_{DS6}^{av} - I_{DS3}^{av}}$$ (V_m)

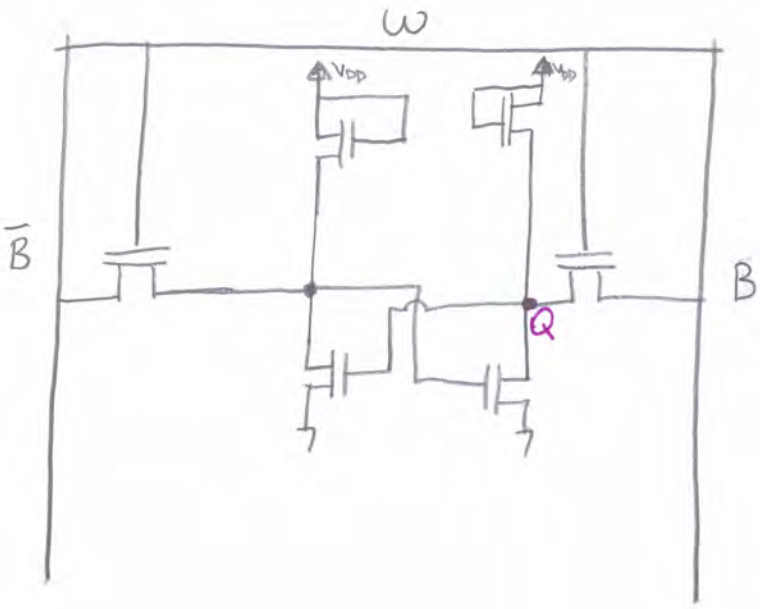
$$V_Q = 0 \Rightarrow I_{DS6,in} = \frac{K_{n6}}{2}\left[V_{DD} - V_{TN}\right]^2$$

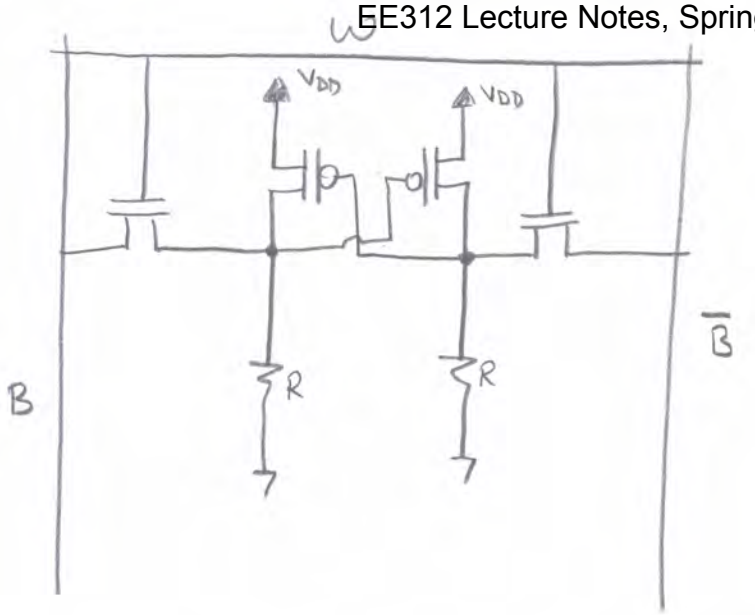
$$I_{DS3,in} = 0$$

$$V_Q = V_{DD}/2 \Rightarrow I_{DS6f} = \frac{K_{n6}}{2}\left[V_{DD}/2 - V_{TN}\right]^2$$

$$I_{DS3f} = K_{n3}\left[\left(\frac{V_{DD}}{2} - V_{TN}\right)\frac{V_{DD}}{2} - \left(\frac{V_{DD}}{2}\right)^2\right]$$

→

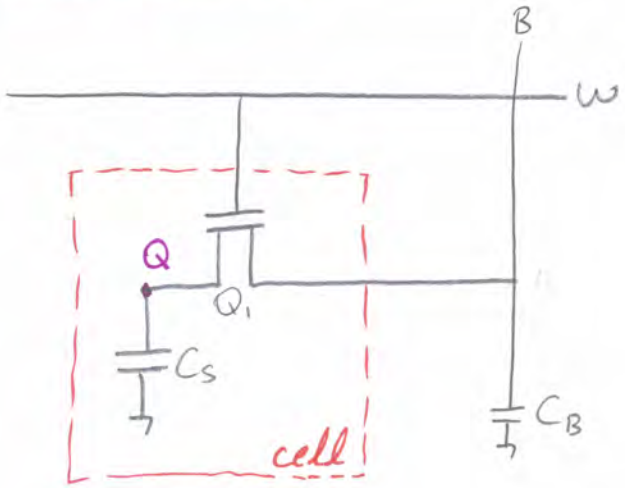




* If Instead of Q_5 we have CMOS:

$$Q_{5n} = \frac{10W}{L}, \quad Q_{5p} = \frac{25W}{L} \left(\text{Initially } Q_5 = \frac{W}{L} \right)$$

Dynamic RAM Cell



* Consider write operation. ("1")

$B = V_{DD}$, $W = V_{DD} \Rightarrow Q = 0 \Rightarrow$ up to $(V_{DD} - V_{TN})$

$$t_{write} = \frac{C_S (V_{DD} - V_{TN})}{I_{DS}}$$

★ Consider read operation (1)

$B = \frac{V_{DD}}{2}$, $C_b \approx 20\text{-}40 \times C_S$

B is connected C_b temperorily and disconnected.

$$\left.\begin{aligned} Q_{CS} &= C_S(V_{DD} - V_{TN}) \\ Q_{CB} &= C_B\left(\frac{V_{DD}}{2}\right) \end{aligned}\right\} \quad \frac{C_S(V_{DD} - V_{TN}) + C_B\frac{V_{DD}}{2}}{C_S + C_B} = \frac{V_{DD}}{2} + \Delta V$$

$$C_S\frac{V_{DD}}{2} - C_S V_{TN} + C_B\frac{V_{DD}}{2} = C_S\frac{V_{DD}}{2} + C_B\frac{V_{DD}}{2} + \Delta V(C_S + C_B)$$

$$\boxed{\Delta V = \frac{C_S\left(\frac{V_{DD}}{2} - V_{TN}\right)}{C_S + C_B}}$$

$\Delta V \geq 10mV$ in order to read.

In fact, sense amplifiers are used to detect ΔV and read.

★ $C_B \leq 149 C_S$ (assumed)

Let us take $C_B = 149 C_S \Rightarrow \Delta V = \frac{C_S(2.5 - 1)}{150 C_S} \Rightarrow \Delta V = 10mV$ ✓ we can sense it.

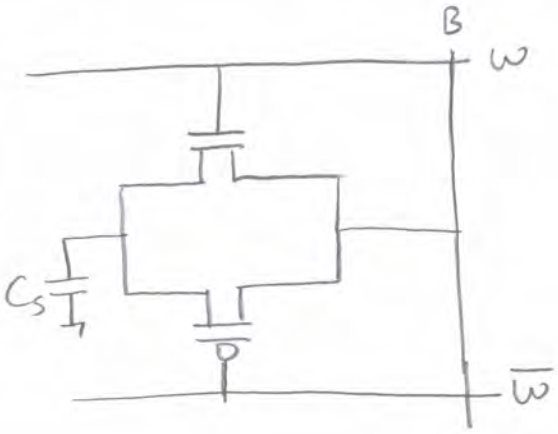
→ If V_{TN} ↓ (assume $V_{TN} = 0$) $\Rightarrow$ $C_B \leq 249 C_S$ to sense (read)
increased

→ If V_{DD} ↗ $\Rightarrow$ C_B/C_S ↗

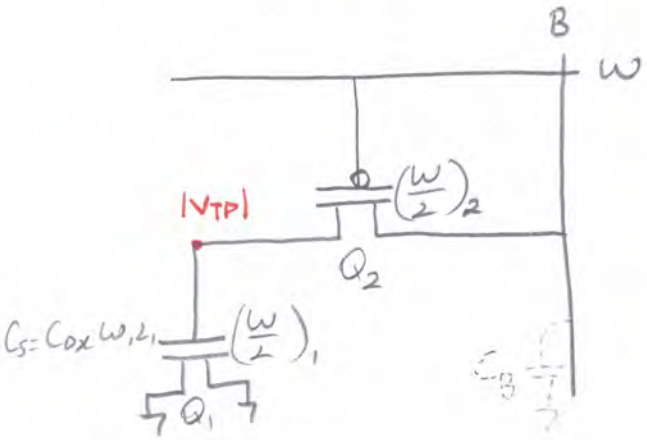
✱ How can we increase C_S/C_B by adding new components or modifying the DRAM?

→ Use depletion transistor.

→ Use CMOS transmission gate.



✱ What should be $(C_S/C_B)_{max}$ for read "0".

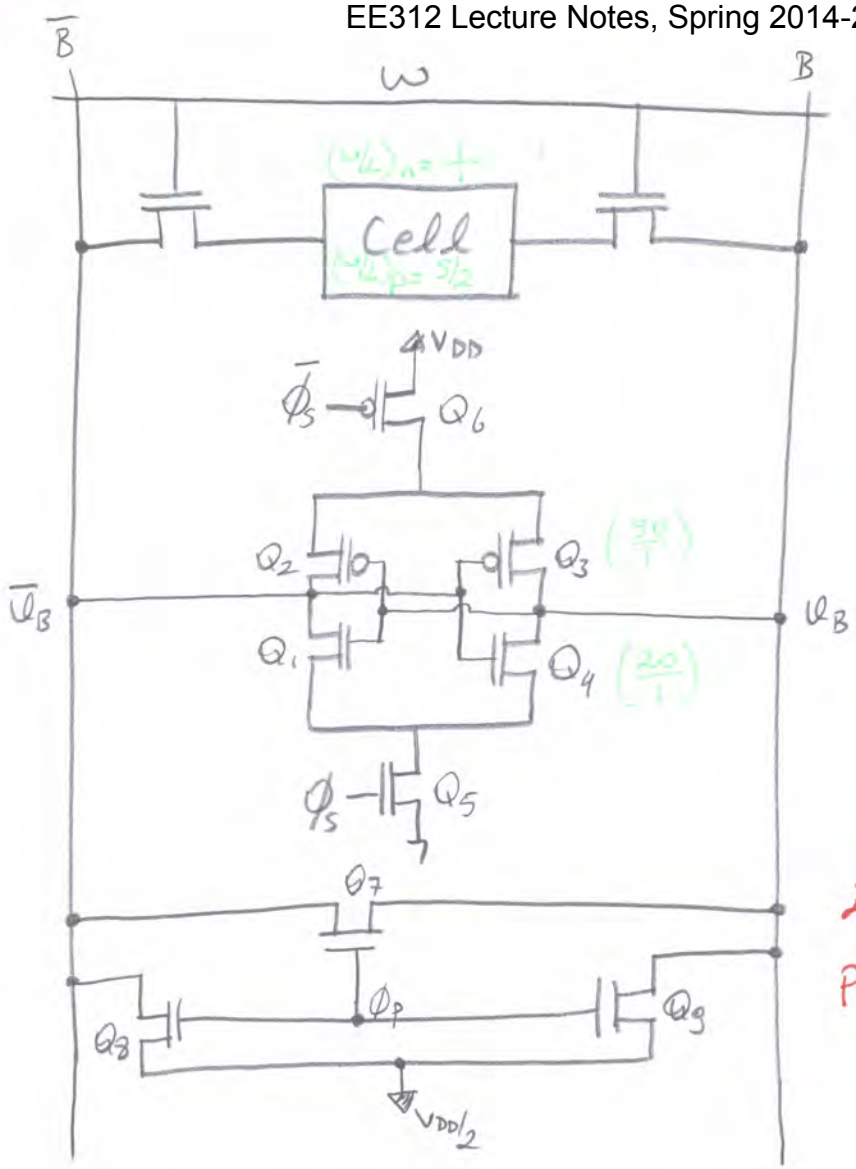


$\Delta V = 10mV$, $t_{read} < 10\mu s$

$$\frac{C_S|V_{TP}| + C_B \frac{V_{DD}}{2}}{C_B + C_S} = \frac{V_{DD}}{2} - \Delta V$$

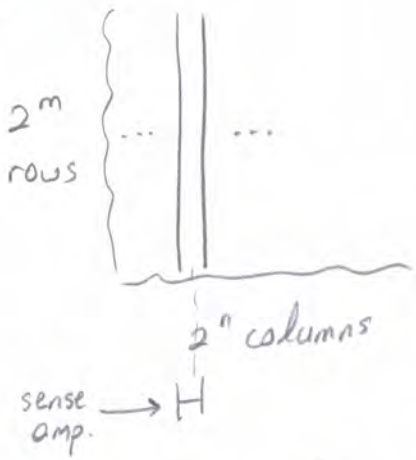
Find (C_S/C_B)

$$\frac{C_S\left(\frac{V_{DD}}{2} - |V_{TP}| - \Delta V\right)}{I_{DQ_2}} = t_{read} < 10\mu s \Rightarrow \text{find } C_S. \Rightarrow \text{find } C_B.$$



Differential Sense Amplifier

Equalization and Precharge Circuitary



$$\text{Power Dissipation} = 2^{m+n} P_{cell} + 2^n P_{sense}$$

We have the following differences between sense amp. and cell.

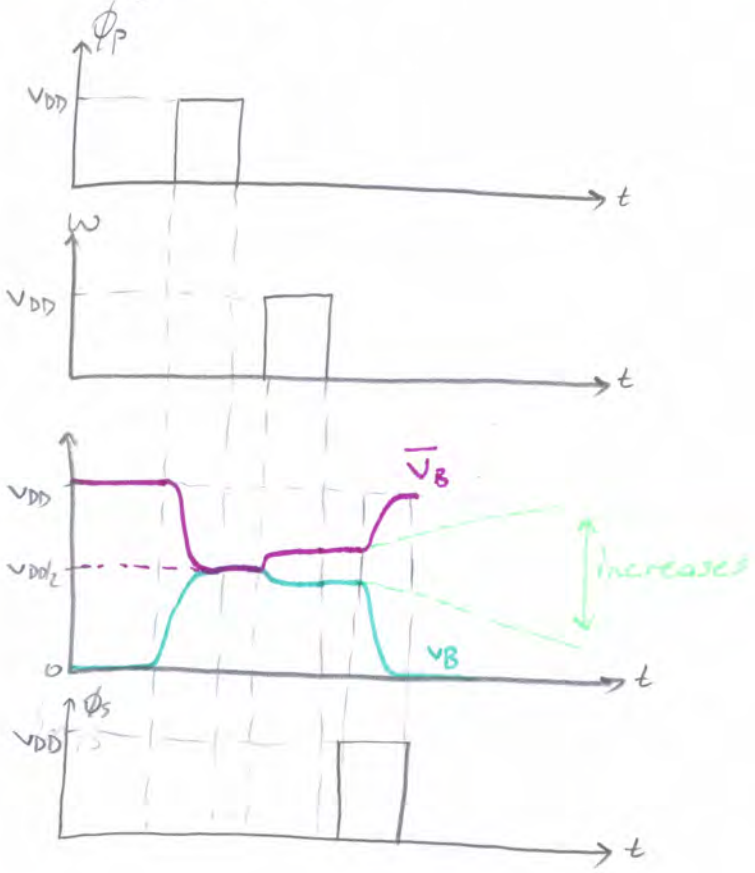
1. Sense amp. is activated with a clock signal.
2. $\left(\frac{W}{L}\right)_{sense} >> \left(\frac{W}{L}\right)_{cell}$.

★ S-RAM Read "0"

→ ϕ_p goes high $\Rightarrow v_B = \bar{v}_B = \frac{V_{DD}}{2}$

→ ϕ_p goes low

→ w goes high



★ $1GB = 10^9 \times 8 byte = 2^{m+n}$

$m+n = 33$

Let $m = 16$

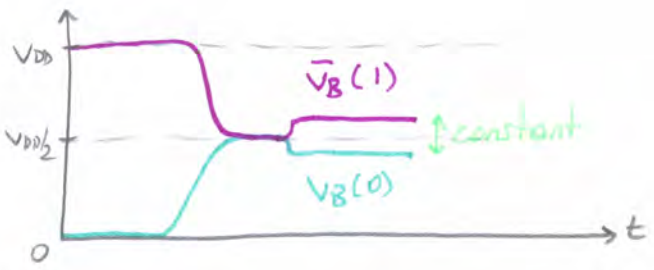
$n = 17$

$\frac{2^{17} \times 1\mu m}{10^3}$ mm

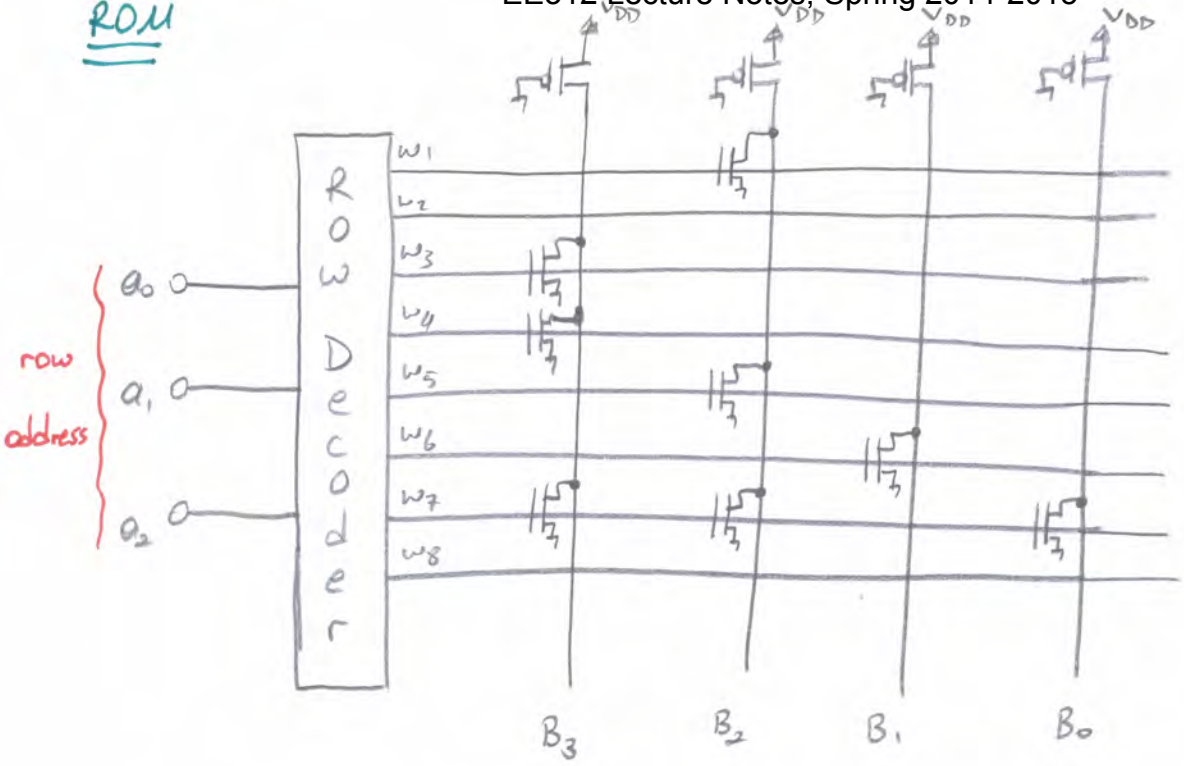
Assume $C_B = 0.5pF/mm$

$\Rightarrow \boxed{C_B = 65.5pF}$

★ D-RAM Read "0"



ROM

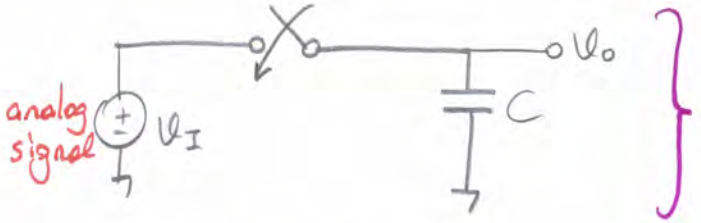


	a_2	a_1	a_2	B_3	B_2	B_1	B_0
w_1	0	0	0	1	0	1	1
w_2	0	0	1	1	1	1	1
w_3	0	1	0	0	1	1	1
w_4	0	1	1	0	1	1	1
w_5	1	0	0	1	0	1	1
w_6	1	0	1	1	1	0	1
w_7	1	1	0	0	0	1	0
w_8	1	1	1	1	1	1	1

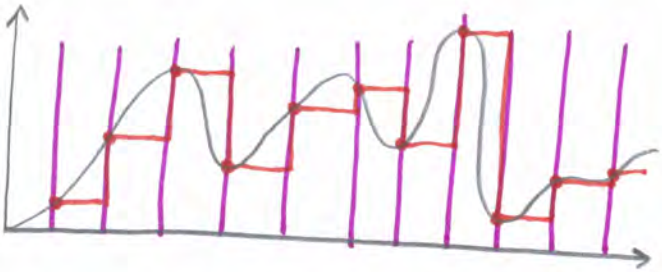
★ There can be more bit lines and this does not change the number of word lines.

★ If the number of 0's in the table is not equal to the number of nmos transistors, our design will be wrong.

Data Converters

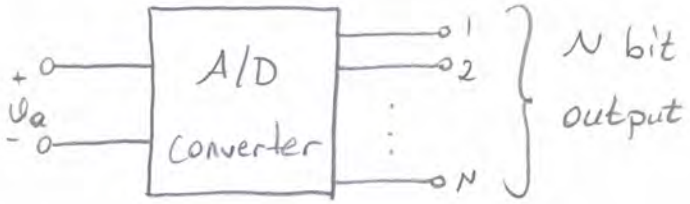


sample and hold circuit



⇒ Analog to Digital Conversion with constant sampling frequency.

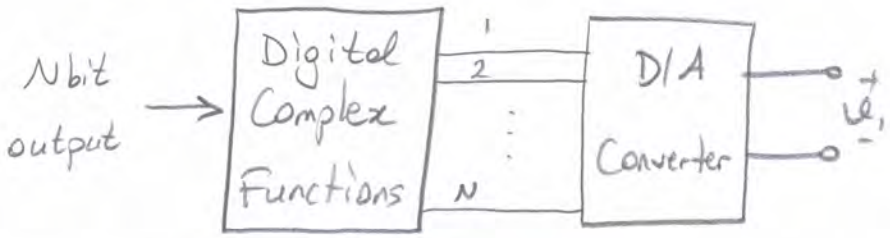
✱ Let us consider A/D converter to observe the general idea.



$\min(v_a) = 0$
$\max(v_a) = 10V$
} Let $n=3 \Rightarrow 2^3 = 8$ levels

$\frac{10-0}{8} = 1.25V$ (each step)

✱ In fact we use converters in order to manipulate analog signals in digital domain. So, we need D/A converters, too.

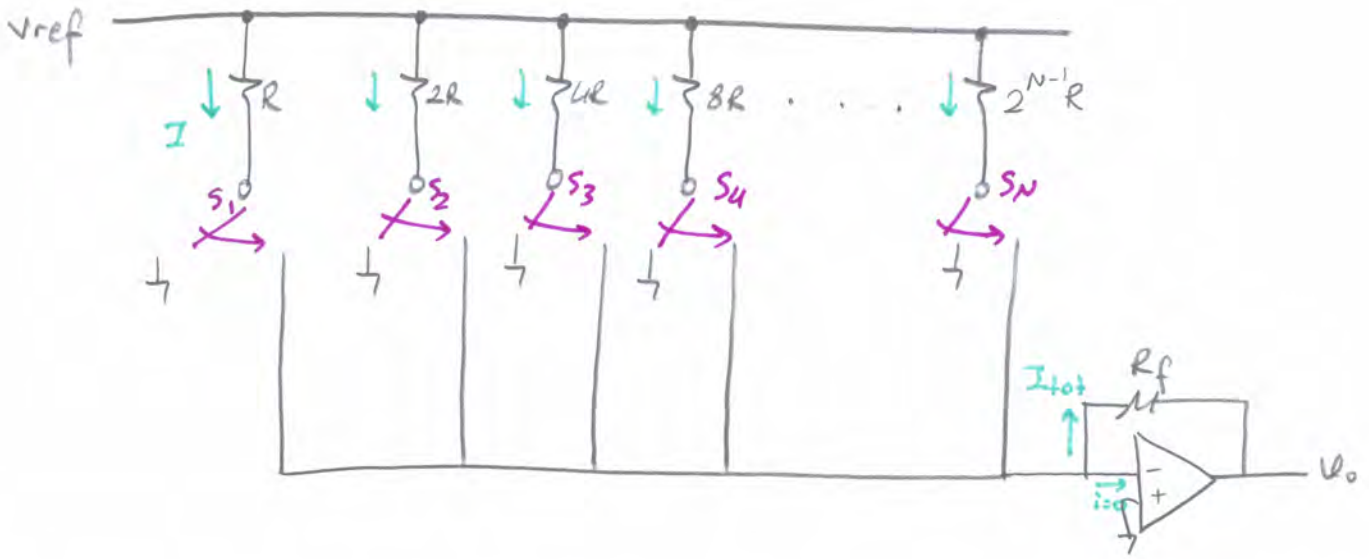


Let $v_a = 2V$ $(n=3)$
We have 001 as output.
This is the input of D/A.
$v_1 = 1.25V \neq 2V$.

This is called quantization error.

$$QE = \frac{max - min}{\quad}$$

D/A Converter



This is called N-bit D/A converter using a binary weighted resistive ladder network.

$$v_o = R_f I_{tot} = V_{ref} \quad \text{(what we want)}$$

$$I_{tot} = \frac{V_{ref}}{R}\underbrace{\left[1 + \frac{1}{2} + \cdots\right]}_{\text{let } N \to \infty} = \frac{V_{ref}}{R/2}$$

$$\Rightarrow v_o = R_f \frac{V_{ref}}{R/2} = V_{ref} \Rightarrow \boxed{R_f = R/2}$$

★ It is clear that if $I_{tot} > 0 \Rightarrow v_o < 0$. However, V_{ref} is always negative $\Rightarrow v_o$ is positive.

★ If we are asked: $V_{ref_{max}} = 10V$

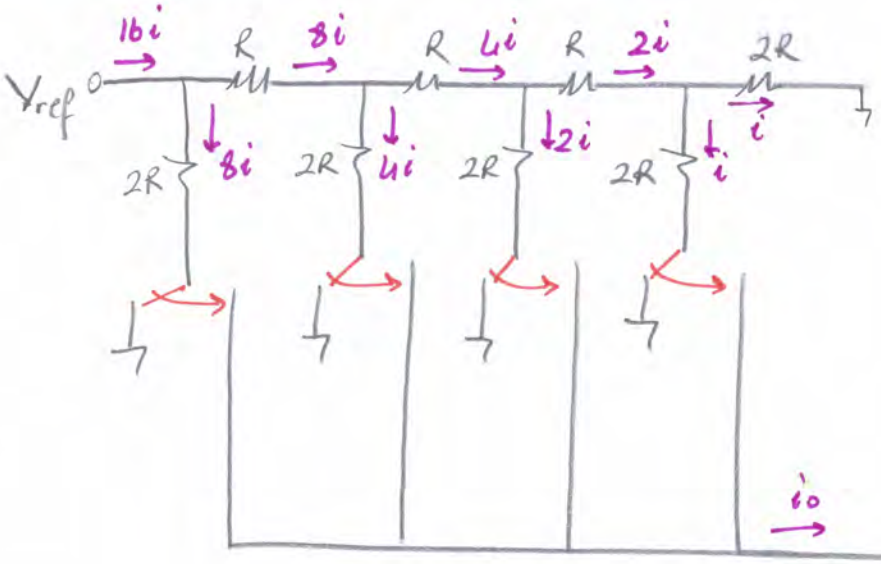
$V_{o_{max}} = 1V$

$$v_o = R_f \frac{V_{ref}}{R/2} \quad (10)$$

$$\boxed{R_f = R/20}$$

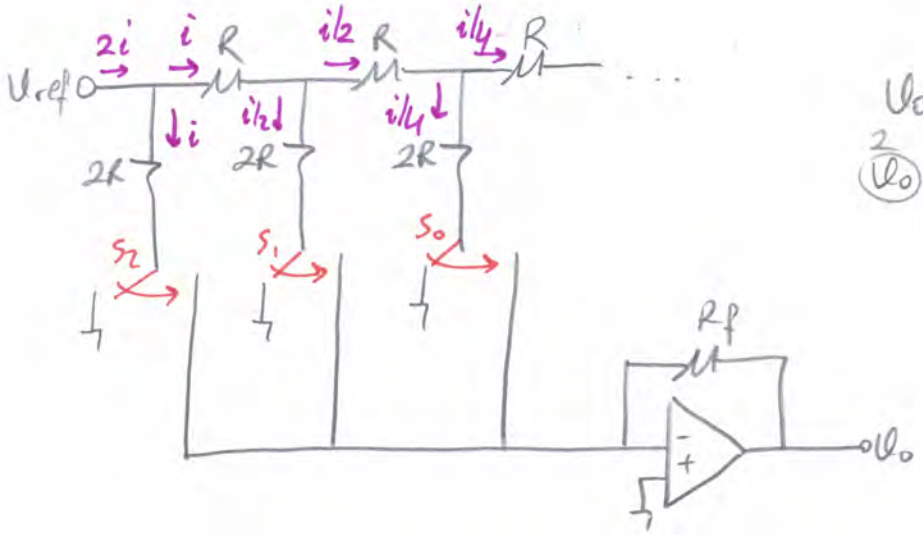
★ If $V_{ref_m} = 10V$, $V_{om} = 10V \Rightarrow$ $\dfrac{\text{max resistance}}{\text{min resistance}} = \dfrac{2^{N-1}R}{R_f} = 2^N$

R-2R Ladder (4-bit)



This design is more convinient for manufacturing.

Ex: Design a 3 bit R-2R ladder to convert the digital signal into analog equivalent using $V_{ref} = -10V$. Analog signal should be [0:2] ($P_d < 10mW$)



$V_o = R_f I_{tot}$

$V_o = R_f \frac{V_{ref}}{R} 10$ (2) $\quad R_f = R/5$

$P_d = V_{ref}(2i)$

$= V_{ref} \not{2} \frac{V_{ref}}{\not{2}R}$

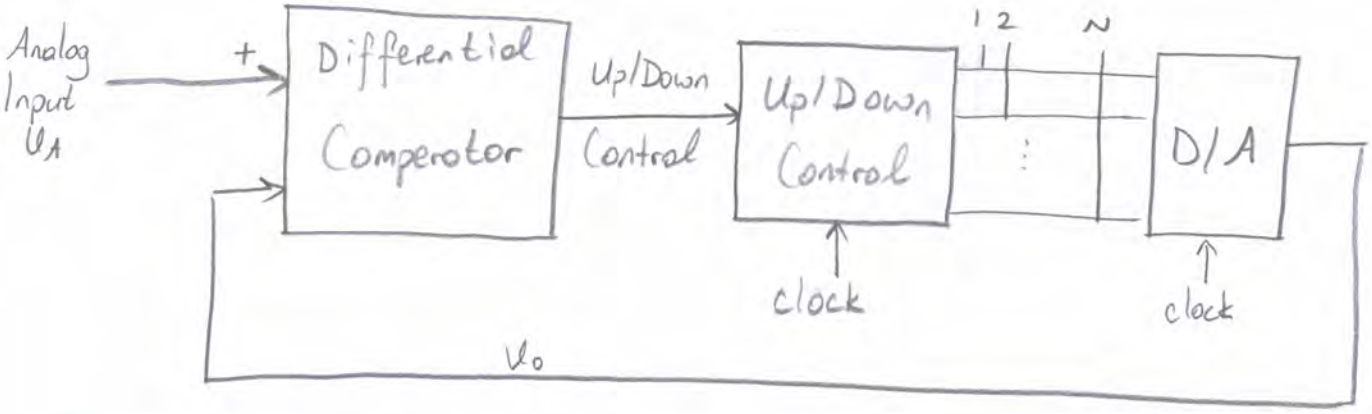
$= \frac{V_{ref}^2}{R} < 10 \times 10^{-3}$

$R > 10k\Omega$

$$+\left(b_2 + b_1\frac{1}{2} + b_0\frac{1}{4}\right)\frac{(+10)\,R_f}{2R\cdot 5} = V_o$$

$$\boxed{V_o = \left(b_2 + \frac{b_1}{2} + \frac{b_0}{4}\right)V}$$

A/D Converter Circuits



- This is a feedback type converter.
- Total conversion time for worst case scenario: $2^N T$
- probability of existance

In that case: $\frac{2^N T}{2}$

- Let $V_A \Rightarrow [0:10]$, $n=7$

  Let $V_A = 2.825V \Rightarrow (11101)_2 \Rightarrow 29T$

  $\frac{10}{2^7} = 0.078125$

  $2.285 / 0.078125$

  29.248

  $(29)_{10} = (11101)_2$ same

- Let $V_A = 7.175V$ in a down control mode.

  29T (the same)

- As $n \nearrow$, time also increases.

D/A Converter Errors

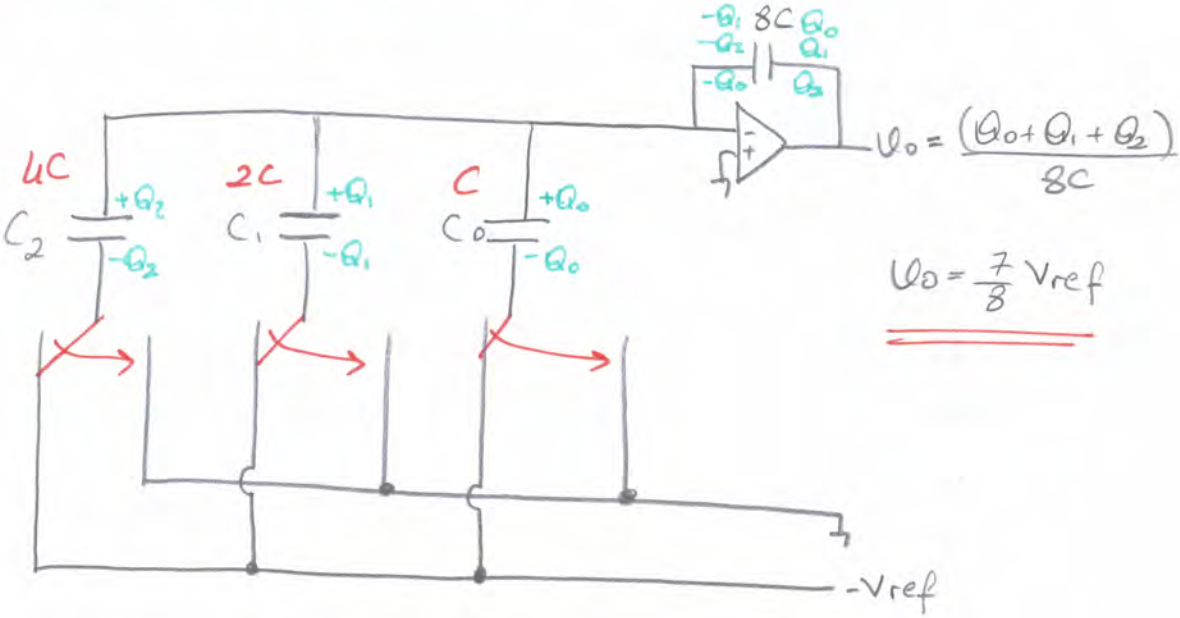
R-2R may vary

$y = mx + n$

m: gain error

n: offset error

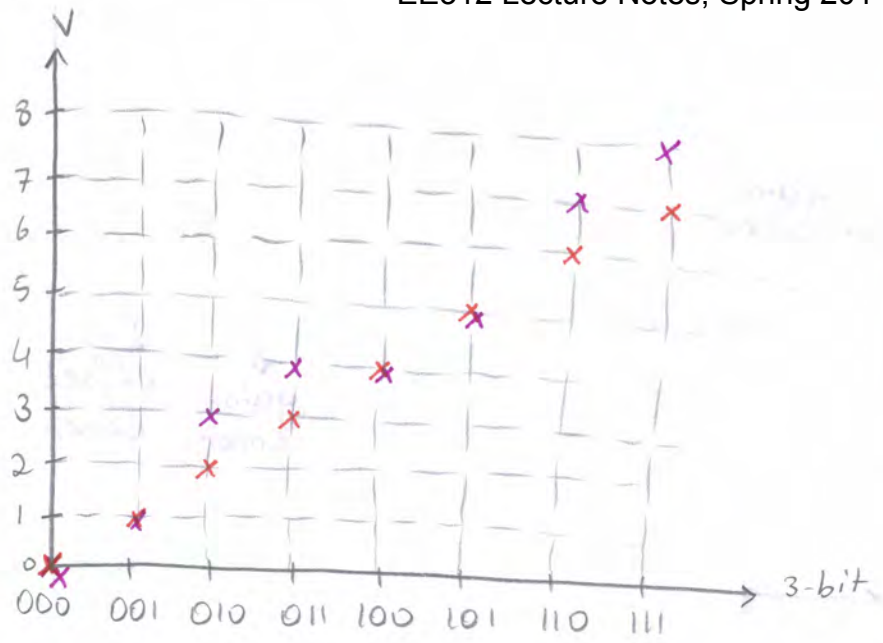
Switched Capacitor D/A



★ If $-2V_{ref} \Rightarrow C_{1new} = C_1/2$ to keep Q unchanged

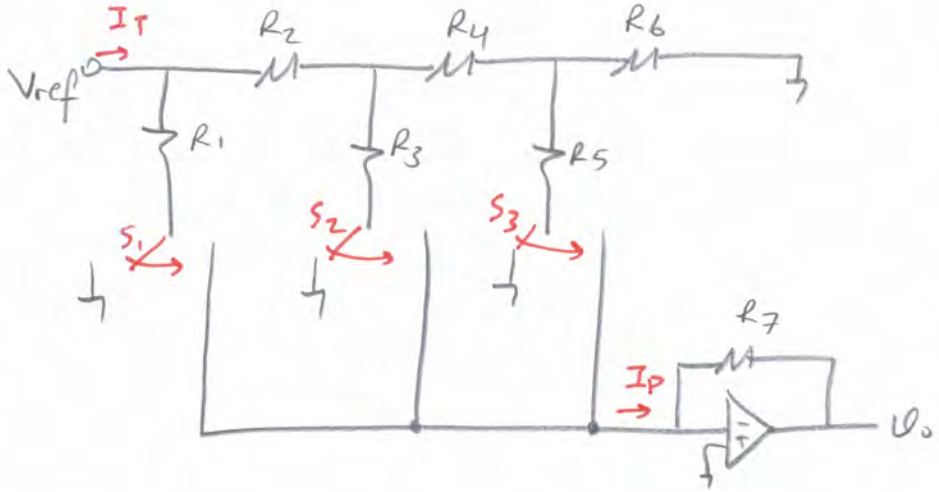
★ Let $C_1 = 3C$ due to errors. ($V_{ref} = 8V$)

b_2	b_1	b_0	ideal analog output	actual analog output
0	0	0	0	0
0	0	1	1	1
0	1	0	2	3
0	1	1	3	4
1	0	0	4	4
1	0	1	5	5
1	1	0	6	7
1	1	1	7	8



	Differential Linearity Error = Actual Step Size − Ideal Step Size	Integral Linearity Error = Actual Output − Ideal Output
000	—	0
001	0	0
010	+1	+1
011	0	+1
100	-1	0
101	0	0
110	+1	+1
111	0	+1

Ex: A 3 bit DAC performing as an ideal converter is given below. The maximum value of I_T current is 1.6mA. Fill in the table with the corresponding values if the total of all resistances is equal to 100kΩ.



Let it be R-2R ladder

$R_1 = R_3 = R_5 = R_6 = 2R$

$R_2 = R_4 = R$

Let $S_1S_2S_3 = 111$

$I_p = 1.4mA$

$U_o = 11.2V$

$R_7 = 8k\Omega$

$10R + R_7 = 100k\Omega$

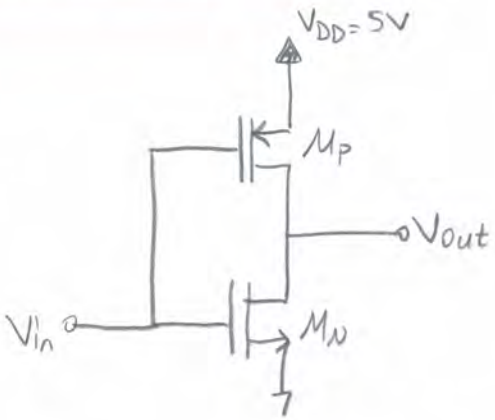
$R = 9.2k\Omega$

$V_{ref} = -RI_T = -14.72V$

Vref(V)	R_1	R_2	R_3	R_4	R_5	R_6	R_7
-14.72	18.4k	9.2k	18.4k	9.2k	18.4k	18.4k	8k

Digital Code $S_1S_2S_3$	I_T(mA)	I_p(mA)	U_o(V) [0:12.8]
000	1.6	0.0	0
001	1.6	0.2	1.6
010	1.6	0.4	3.2
011	1.6	0.6	4.8
100	1.6	0.8	6.4
101	1.6	1.0	8
110	1.6	1.2	9.6
111	1.6	1.4	11.2

EE312 MT2 Q2



M_N
$K_N = 100\mu A/V^2$
$V_{TN} = 0V$
$\lambda = 0$

M_P
$K_P = 25\mu A/V^2$
$V_{TP} = 0$
$\lambda = 0$

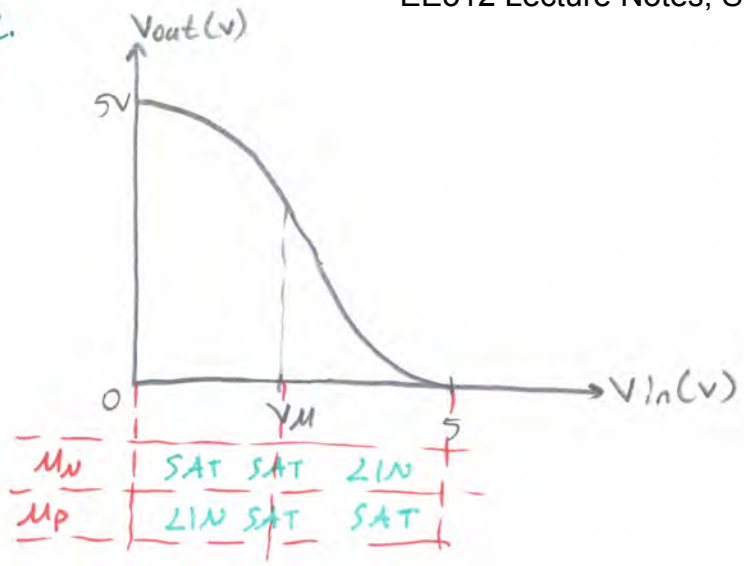
a. Sketch the VTC. Clearly label the operation mode of transistors in each region.

b. Calculate f_{max} for this inverter to be successfully operated with an input signal of 50% duty cycle between V_{OL} and V_{OH} for a maximum fanout of 10. Each inverter has an input capacitance of 1pF.

c. Implement the following function Y using a CMOS gate and an enable signal E. When E=1, Y should implement the given function. When E=0, Y should be high-z. Inverted signals are available.

$$Y = \overline{(A + BC)D}$$

a.



$V_{OH} = 5V$

$V_{OL} = 0V$

At V_M both in SAT

$\frac{1}{2} K_n (V_M - 0)^2 = \frac{1}{2} K_p (5 - V_M)^2$

$4 V_M^2 = (5 - V_M)^2$

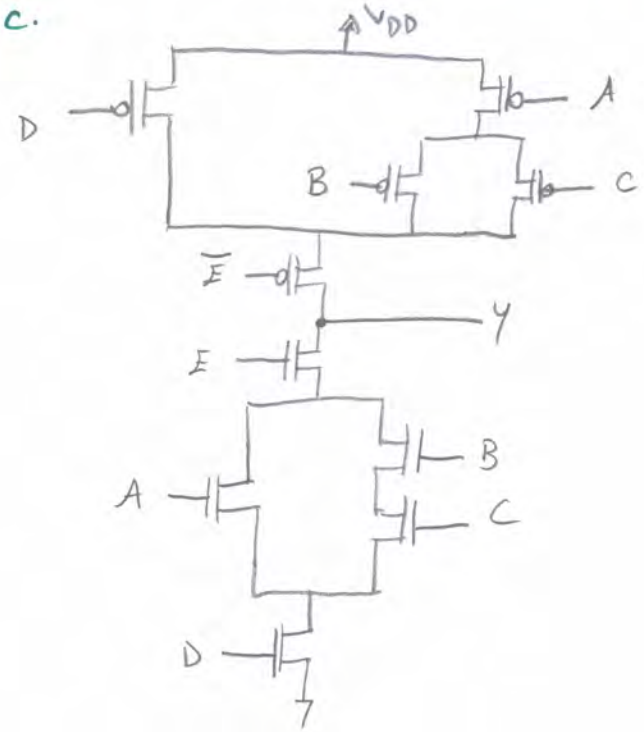
$V_M = 1.66V$

b. $I_{dis} = \frac{1}{2} K_n (5-0)^2 = 1.25mA \Rightarrow t_{dis} = \frac{5 \times 10 \times 10^{-12}}{1.25 \times 10^{-3}} = 40ns$

$I_{ch} = \frac{1}{2} K_p (5-0)^2 = 0.3125mA \Rightarrow t_{ch} = \frac{5 \times 10 \times 10^{-12}}{0.3125 \times 10^{-3}} = 160ns$

$$f = \frac{1}{2 \times 160ns} = 3.125MHz$$

c.



EE312 MT2 Q3

a. Implement the following function X using pass transistor logic having only PMOS transistors. Complementary inputs are available.

$$X = A(B+C)$$

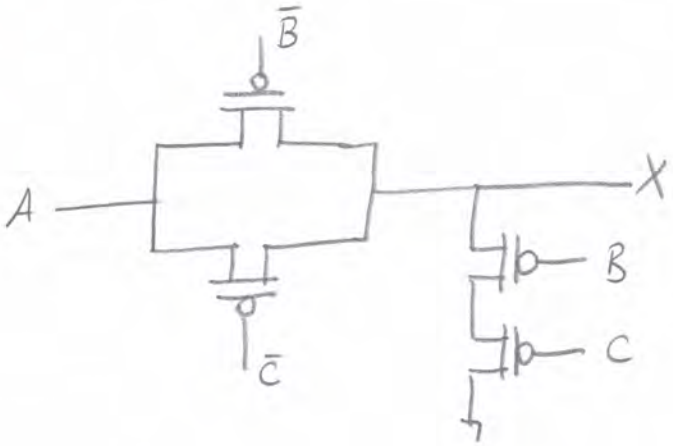
b. Implement the following function Y using dynamic logic with a single stage. Complementary inputs are available.

$$Y = AB(C+D)$$

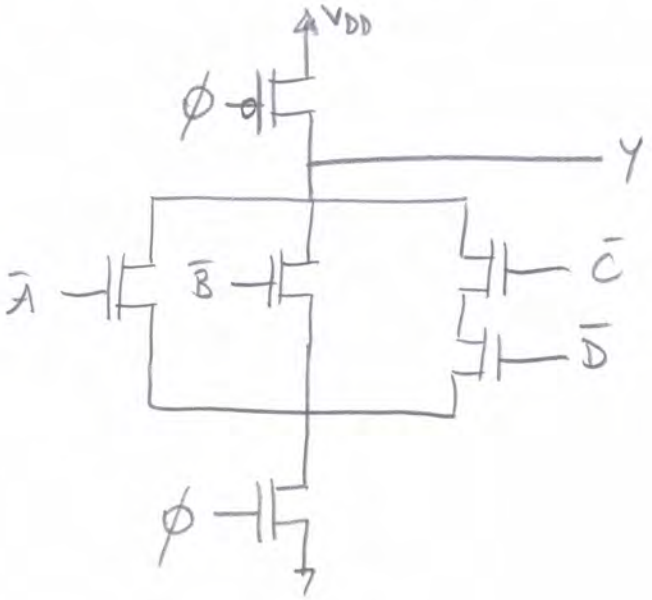
c. If the number of inputs per logic gate is limited to at most 4, implement the following function Z using domino logic. You can use multiple gates. Complementary inputs are available.

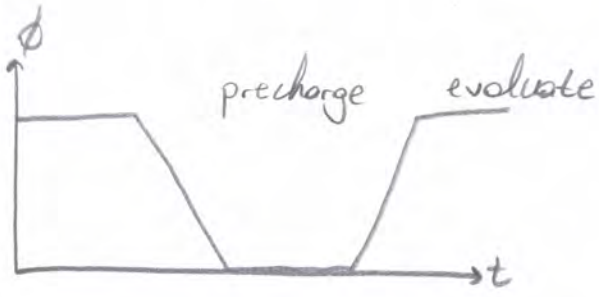
$$Z = \overline{ABC + ABD} + (C+DE)$$

a.



b. $Y = \overline{\overline{AB(C+D)}} = \bar{A} + \bar{B} + \bar{C}\bar{D}$

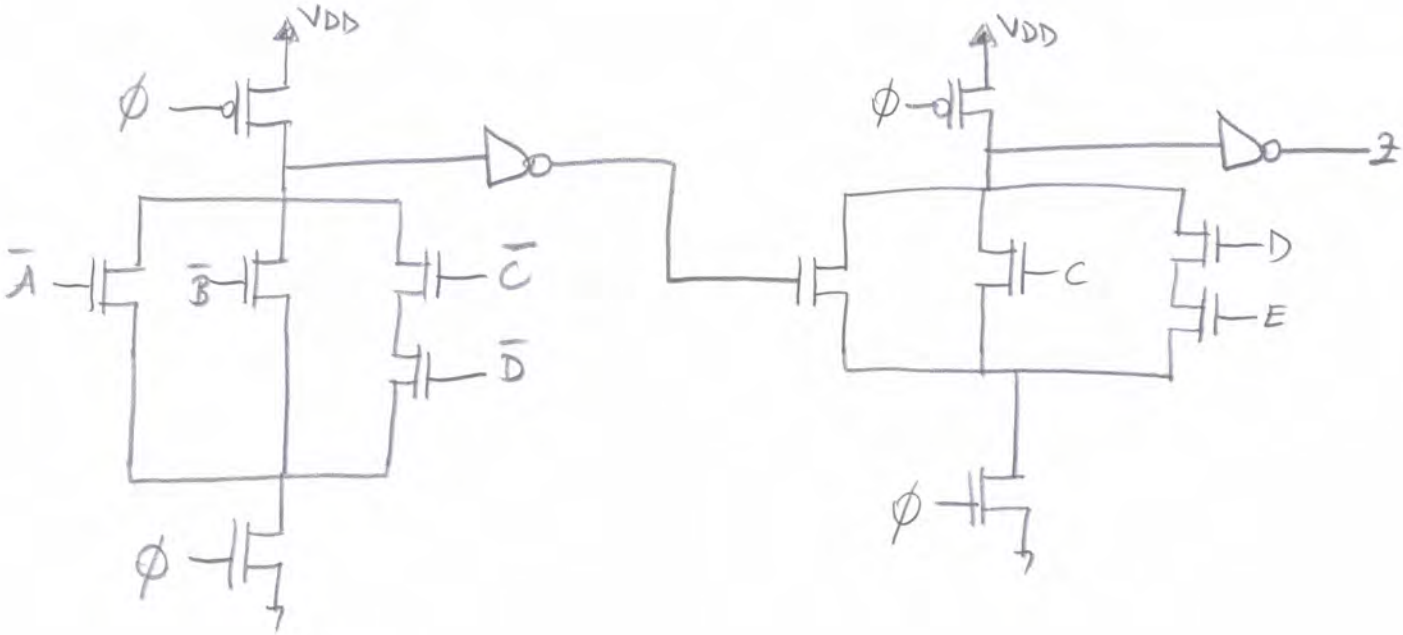




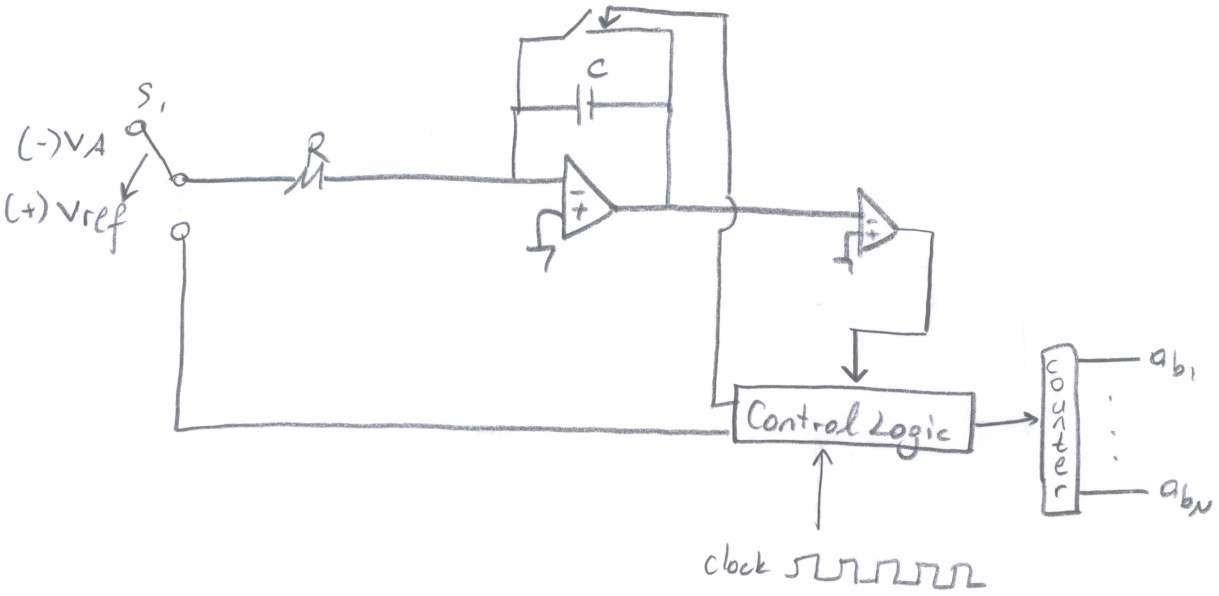
c. $Z = \overline{AB(C+D)} + (C + DE)$

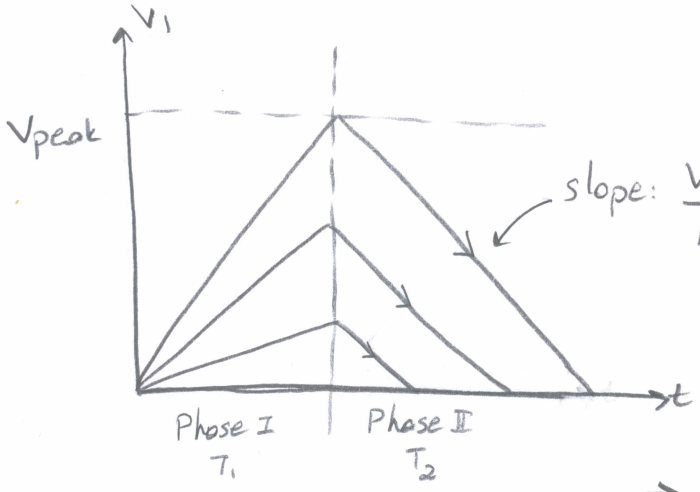
$= F + C + DE$

$F = \overline{AB(C+D)} \Rightarrow \bar{F} = \bar{A} + \bar{B} + \bar{C}\bar{D}$



Dual Slope Converter



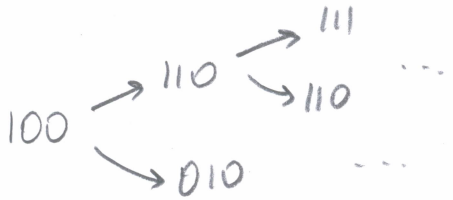


$$V_{peak} = \frac{V_{ref}}{RC} T_1$$

$$T_2 = V_{peak} \frac{RC}{V_{ref}}$$

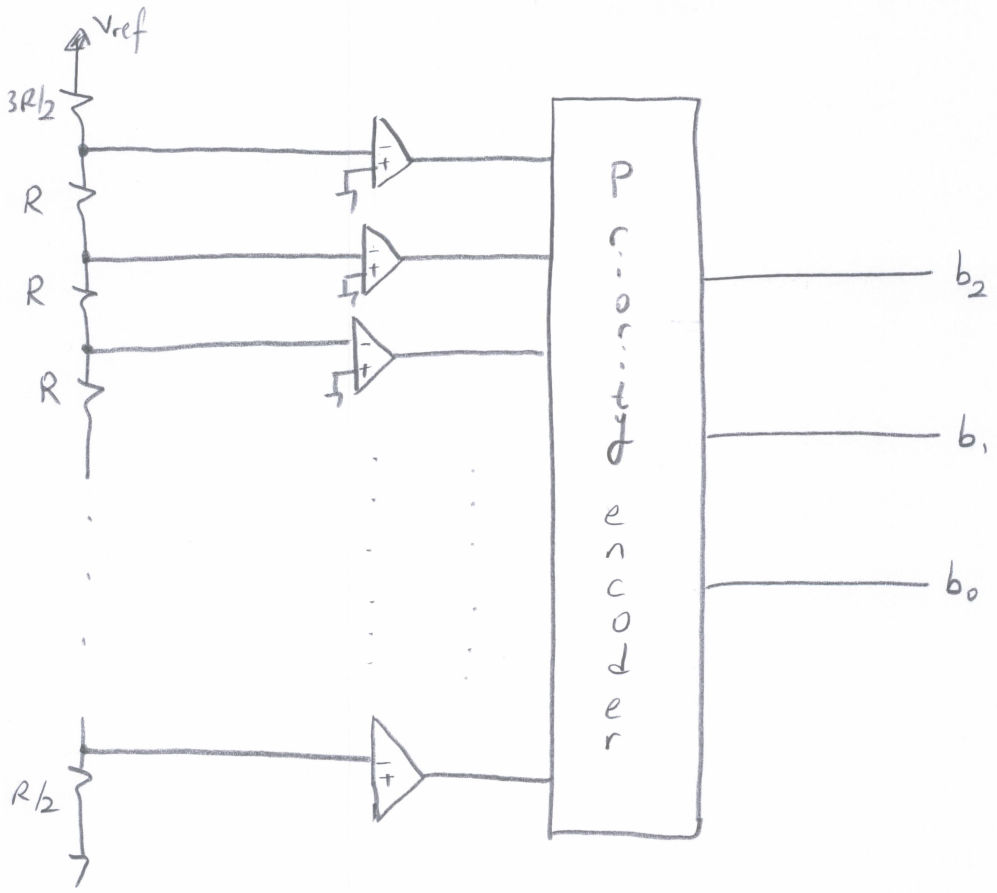
$$\Rightarrow \boxed{\frac{V_A}{V_{ref}} = \frac{T_2}{T_1}}$$

Successive Approximation



In that case, instead of $2^n T$ time (in worst case), we have nT time in worst case.

Flash Converter



In worst case, it takes one clock cycle.

April 16, 2015 at 11:20 am in EA-312

Göktuğ Cihan Özmen,

Taking class notes meticulously

as a volunteer for his classmates.