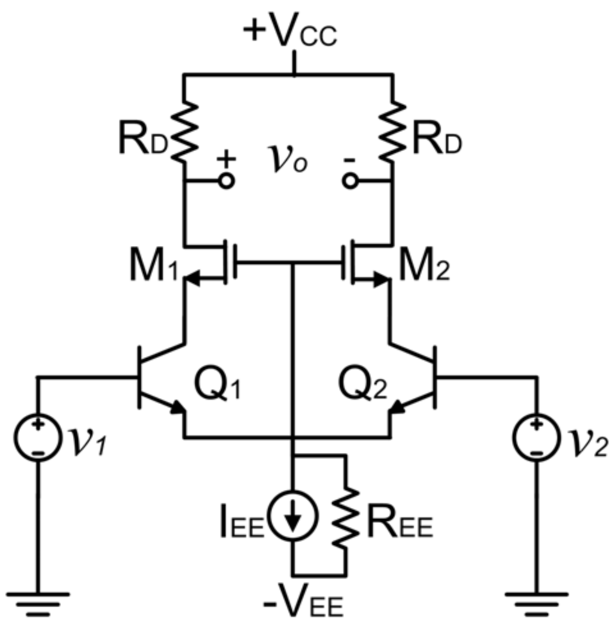
EE311 Analog Electronics #4

Q1) For the differential amplifier given in the figure;



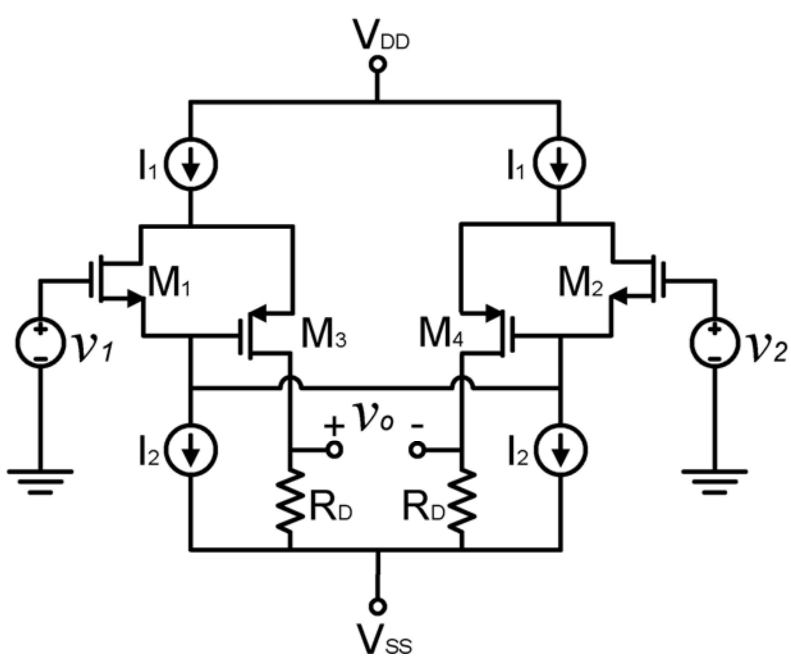
Q_1-Q_2 parameters
$\beta = 100$
$V_A = \infty$
$V_T = 25$ mV
$V_{BE(on)} = 0.7$ V

M_1-M_2 parameters
$K_n = 0.2$ mA/V^2
$V_{TN} = -4$ V
$V_A = \infty$

$V_{CC} = 15$ V
$V_{EE} = 15$ V
$I_{EE} = 100$ µA
$R_D = 75$ kΩ
$R_{EE} = 600$ kΩ

a) Find the DC values (I_C,V_{CE}) of Q_1 and (I_D,V_{DS}) of M_1 transistors.
b) Find the differential-mode gain.
c) Find the common-mode gain.
d) Find the differential mode input resistance.

Q2) For the differential amplifier given in the figure;



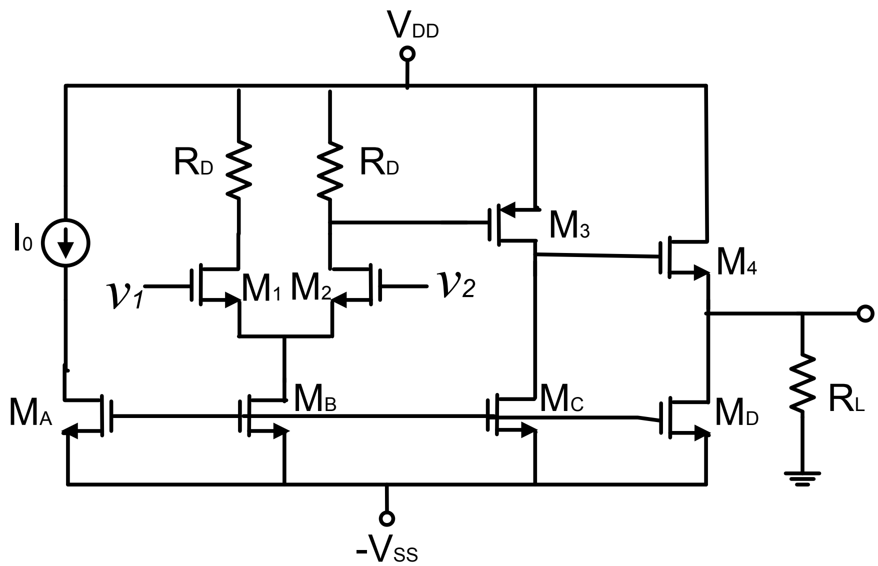
NMOS
$V_{TN} = 0.75$ V
$\mu_n C_{ox}(W/L) = 1$ mA/V^2

PMOS
$V_{TP} = -0.75$ V
$\mu_p C_{ox}(W/L) = 0.5$ mA/V^2

$V_{DD} = 1.5$ V
$V_{SS} = -1.5$ V
$I_1 = 0.2$ mA
$I_2 = 0.1$ mA
$R_D = 10$ kΩ

a) Find the DC drain current (I_D) and the small signal parameter g_m of the M_1 and M_3 transistors.
b) Draw the small-signal equivalent circuit model for the differential mode.
c) Find the differential-mode gain.
d) Find the common mode input range, assuming that a minimum voltage drop of 0.1V across the current sources is required.

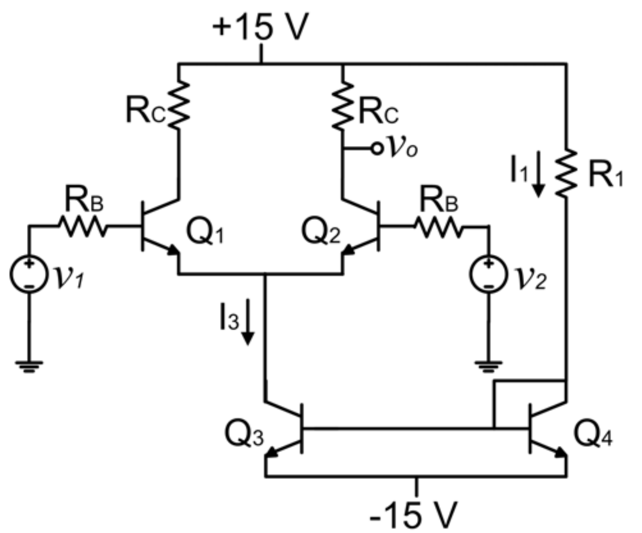
Q3)



$I_0 = 200$ uA
$K_{nB} = K_{nA}$
$K_{nC} = 2.5\ K_{nA}$
$K_{nD} = 25\ K_{nA}$
$K_{n1} = K_{n2} = K_{n4} = 5mA/V^2$
$K_{p3} = 2.5\ mA/\ V^2$
$V_{tp} = -1$ V
$R_L = 2\ k\Omega$
$r_{oMb} = 375\ k\Omega$
$r_{oM3} = 200\ k\Omega$
* The r_o's for the other transistors are infinitely large.
* M_A, M_B, M_C, M_D, have same V_t values but different K_n values.

a) Calculate the bias current of each transistor in the circuit. Neglect the early effect in DC calculations.
b) What is the overall differential mode voltage gain?

Q4) In the BJT differential amplifier in the figure, v_1 and v_2 are AC sources.



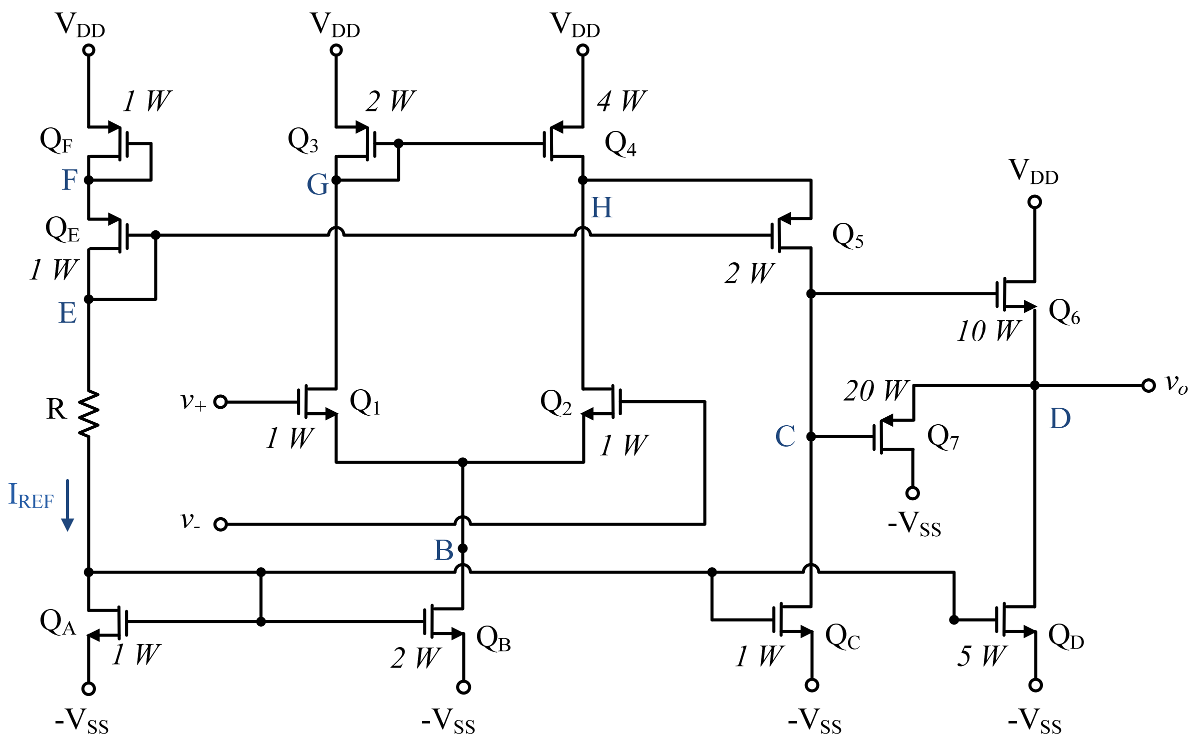
$V_{BE(on)}$ = 0.7 V
β =100
R$_B$=10 kΩ

<u>For Q_1-Q_2 matched pair</u>:
V$_A$ = ∞

<u>For Q_3-Q_4 matched pair</u>:
V$_A$ = 50 V

a) Find the resistance values for R_C and R_1 if I_3=400 μA and $V_{CE1}=V_{CE2}$=10 V. Assume $V_A=\infty$ for all transistors in DC calculations. Also neglect the base currents.
b) Determine the differential mode gain $A_{dm}=v_o/(v_1-v_2)$ and the common mode gain $A_{cm}=v_o/v_{cm}$, $v_{cm}=v_1=v_2$. Draw the half-circuits for the differential mode and the common mode.
c) Determine the differential mode input resistance R_{id} and the common mode input resistance R_{icm}.

Q5)

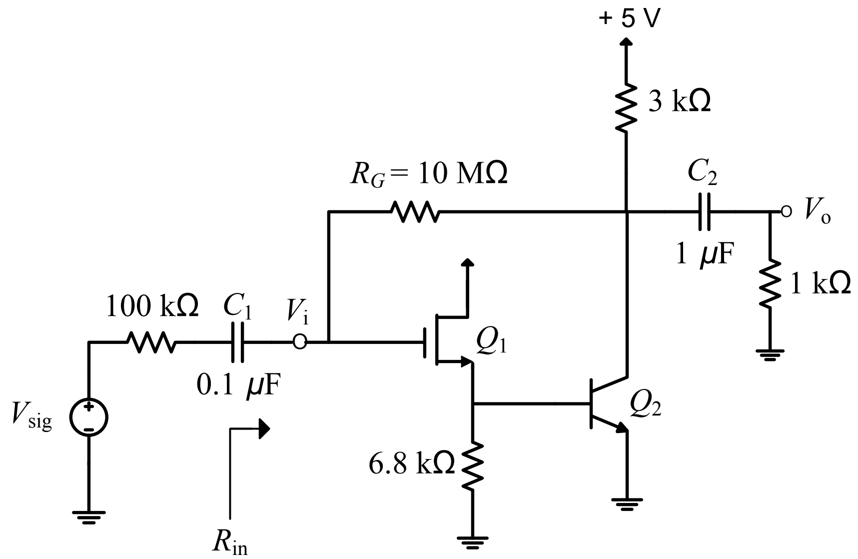


For All MOS devices:
$|V_t| = 1$ V
$\mu_n C_{ox} = 40\ \mu A/V^2$
$\mu_p C_{ox} = 20\ \mu A/V^2$
$|V_A| = 50$ V
L = 5 μm
W = 5 μm

$V_{DD} = 5$ V
$V_{SS} = 5$ V

a) Design R to provide a 10 μA reference current.
b) Calculate the voltage gain $v_o/(v_+ - v_-)$, the input resistance, and the output resistance.
c) What is the input common-mode range?
d) For what load resistance connected to ground is the output negative voltage limited to -1 V before Q_7 begins to conduct?

Q6)

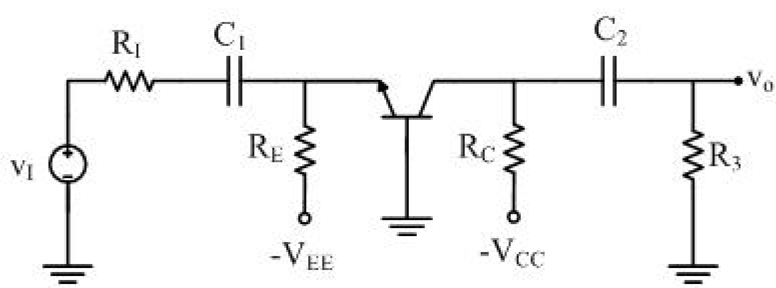


BJT
$|V_{BE}| = 0.7$ V
$\beta = 200$
$C\mu = 0.8$ pF
$f_T = 600$ MHz

NMOS
$V_t = 1$ V
$k'_n W/L = 2 \text{mA/V}^2$
$C_{gs} = C_{gd} = 1$ pF

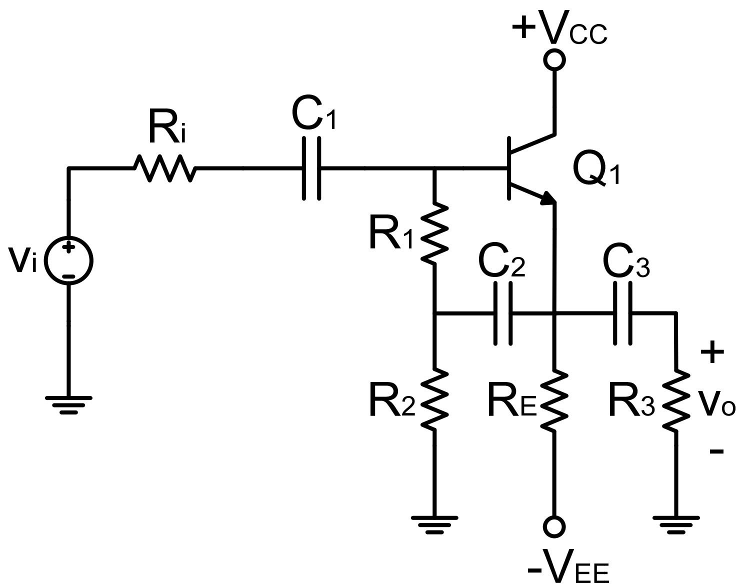
a) Consider the dc bias circuit. Neglect the base current of Q_2 in determining the current in Q_1, find the dc bias currents in Q_1 and Q_2, and show that they are approximately 100 µA and 1 mA respectively.
b) Determine the overall voltage gain V_o/V_{sig}.
c) Estimate the lower 3-dB frequency, f_L.
d) Estimate the higher 3-dB frequency, f_H.
e) To considerably reduce the effect of R_G on R_{in} and hence on amplifier performance, consider the effect of adding another 10 MΩ resistor in series with the existing one and placing a large bypass capacitor between their joint node and ground. What will R_{in}, A_M and f_H become? Explain briefly.

Q7) Find the upper-cutoff frequency of the common-drain amplifier.



R_I = 200 Ω
R_E = 4.3 kΩ
R_C = 2.2 kΩ
R_3 = 51 kΩ
β = 100
r_x = 300 Ω
f_T = 500 GHz
$C\mu$ = 0.6 pF
Q-point (1 mA, 5 V)
$r_o = \infty$

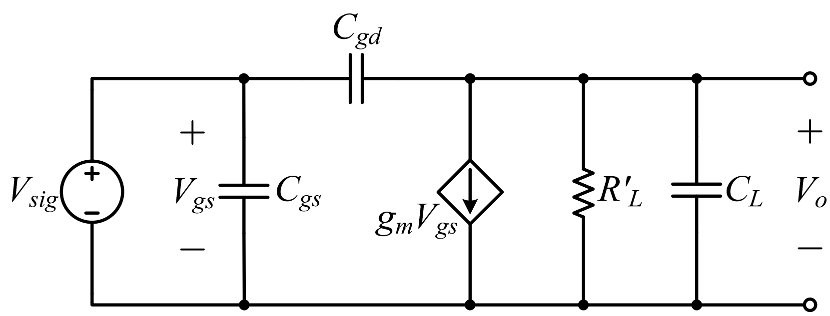
Q8) What are the voltage gain A_V and the maximum input signal amplitude for the amplifier in the figure?



For the BJT, Q_1
$\beta_F = 100$
$V_A = 60$ V

$R_i = 500\ \Omega$
$R_1 = 500\ k\Omega$
$R_2 = 500\ k\Omega$
$R_3 = 500\ k\Omega$
$R_E = 430\ k\Omega$
$V_{CC} = 9$ V
$V_{EE} = 9$ V

Q9) The figure below shows the equivalent circuit when the CS amplifier is fed with an ideal source V_{sig} having $R_{sig} = 0$. Note that C_L denotes the total capacitance at the output node.



$C_{gd} = 0.5$ pF
$C_L = 2$ pF
$g_m = 4$ mA/V
$R'_L = 5\ k\Omega$

a) By writing a node equation at the output, show that the transfer function V_o/V_{sig} is given by

$$\frac{V_o}{V_{sig}} = -g_m R'_L \frac{1 - s(C_{gd}/g_m)}{1 + s(C_L + C_{gd})R'_L}$$

b) At frequencies $\omega \ll (g_m/C_{gd})$, the s term in the numerator can be neglected. In such case, what is the upper 3-dB frequency resulting? Compute the values of A_m and f_H.