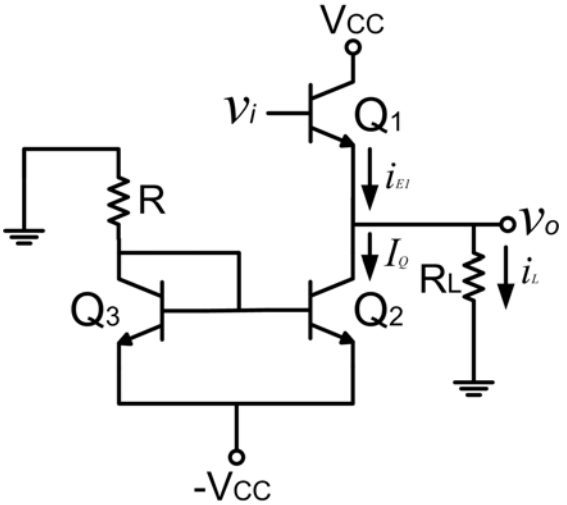
10/06/2010
Spring 2010

EE311 Analog Electronics
Final

Q1) (15 pts.) A class-A emitter follower biased with a constant current source is given in the figure. You can neglect the base currents in your calculations.



$V_{CC} = 10$ V
$R_L = 1$K
$\beta = 200$
$V_{BE(on)} = 0.7$ V
$V_{CE(sat)} = 0.2$ V
$V_{BE(sat)} = 0.8$ V

a) Determine the value of R that will produce the maximum possible output signal swing. What is the value of I_Q, and the maximum and minimum values of i_{E1} and i_L?

b) Using the results of part (a), calculate the conversion efficiency.

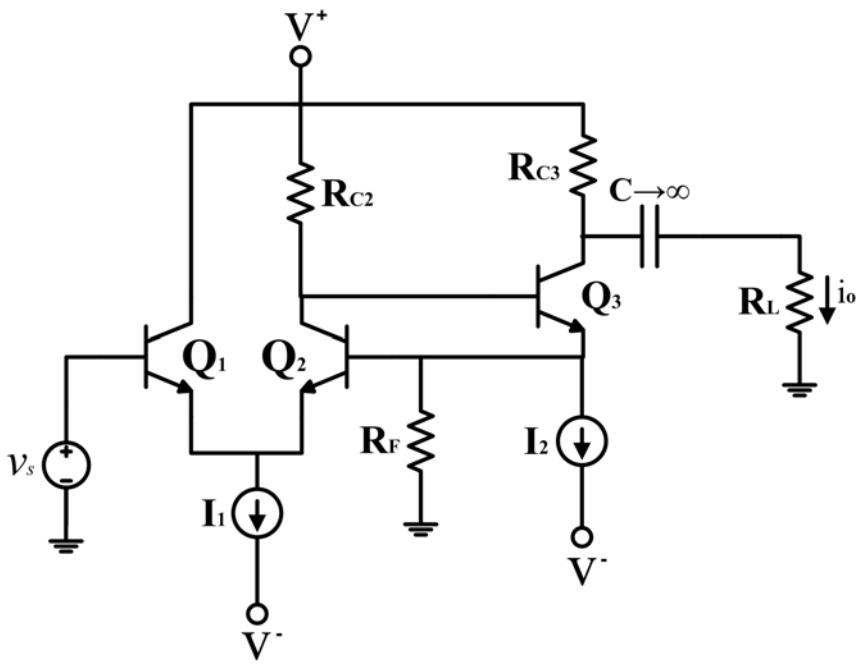
Q2) (15 pts.) Consider a three-pole feedback amplifier with a loop gain function given by

$$T(f) = \frac{\beta \times 1000}{\left(1 + j\frac{f}{10^3}\right)\left(1 + j\frac{f}{5 \times 10^4}\right)\left(1 + j\frac{f}{10^6}\right)}$$

a) Determine the value of β that yields a phase margin of 45 degrees. What is the value of closed loop low frequency gain for this case?

b) If β is changed to 0.14, determine the new closed loop low frequency gain and the approximate phase margin.

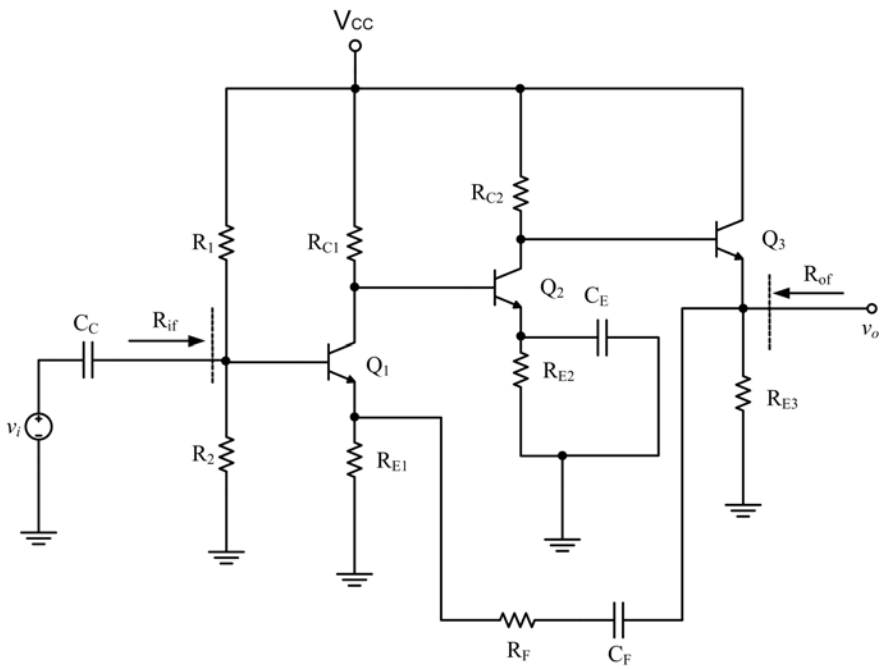
Q3) (15 pts.) A transconductance (series-series) amplifier is given in the figure. Calculate the closed loop transconductance gain $A_{gf}=i_o/v_s$.



$V^+ = 10$ V
$V^- = -10$ V
$\beta = 100$
$V_{BE(on)} = 0.7$ V
$V_A = \infty$
$R_F = 10K$
$R_{C2} = 18.6K$
$R_{C3} = 2K$
$R_L = 1K$
$I_1 = 1$ mA
$I_2 = 2$ mA

Q_1, Q_2, Q_3 parameters
$g_{m1}=g_{m2}=19.23$ mA/V
$r_{\pi 1}= r_{\pi 2}=5.2$ K
$g_{m3} =76.92$ mA/V
$r_{\pi 3} =1.3$ K

Q4) (25 pts.) For the given series-shunt feedback circuit,



V_{CC} = 10 V
β = 120
$V_{BE(on)}$= 0.7 V
$V_A = \infty$
R_1 = 400 kΩ
R_2 = 75 kΩ
R_{C1} = 8.8 kΩ
R_{E1} = 0.5 kΩ
R_{C2} = 13 kΩ
R_{E2} = 3.6 kΩ
R_F = 10 kΩ
R_{E3} = 1.4 K
C_C, C_E, $C_F \rightarrow \infty$

Q_1, Q_2, Q_3 parameters

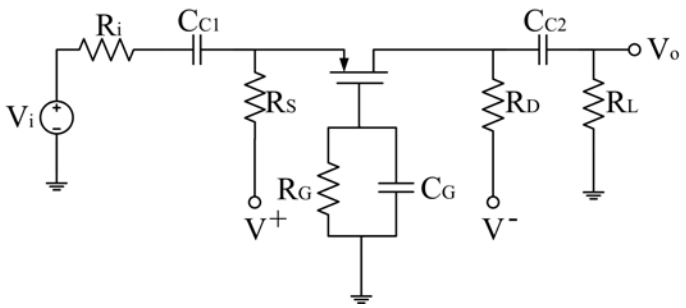
g_{m1} =32.81 mA/V
$r_{\pi 1}$ =3.66 K
g_{m2} =19.12 mA/V
$r_{\pi 2}$ =6.28 K
g_{m3} =78.08 mA/V
$r_{\pi 3}$ =1.54 K

a) Determine the closed loop voltage gain $A_{vf}=v_o/v_i$.

b) Determine the input resistance R_{if}.

c) Determine the output resistance R_{of}.

Q5) (15 pts.) For the common gate amplifier in the figure,

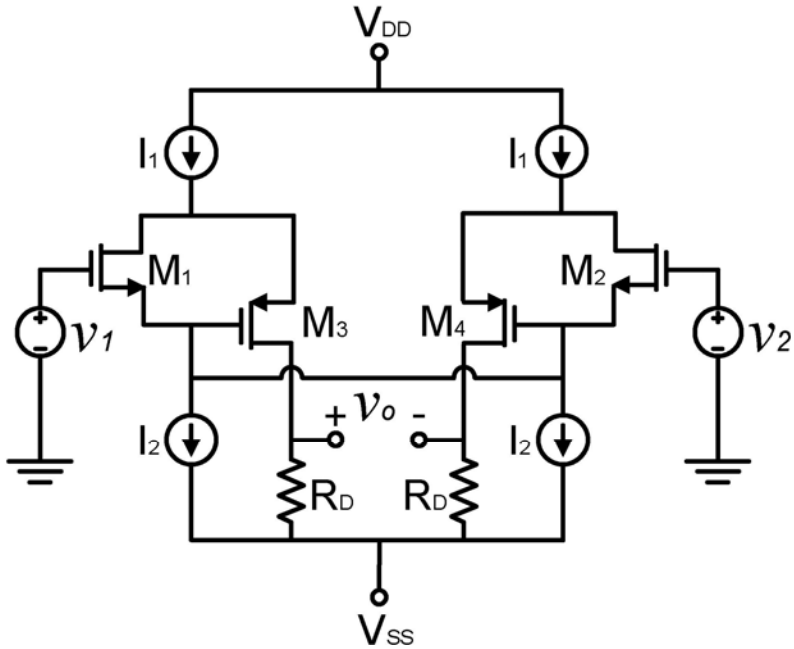


$V^+ = 5$ V
$V^- = -5$ V
$R_S = 4K$
$R_D = 2K$
$R_L = 4K$
$R_G = 50K$
$R_i = 0.5K$

PMOS
$K_p = 1$ mA/V²
$V_{TP} = -0.8$ V
$\lambda = 0$
$C_{gs} = 4$ pF
$C_{gd} = 1$ pF

a) Determine the midband voltage gain $A_v = v_o/v_i$.
b) Determine the upper 3 dB frequency.

Q6) (15 pts.) A differential amplifier will be designed using the given topology in the figure.



V_{DD} = 6 V
V_{SS} = − 6 V

NMOS:
V_{TN} = 1 V
$\mu_n C_{ox}(W/L)$ =1 mA/V^2

PMOS:
V_{TP} = - 1 V
$\mu_p C_{ox}(W/L)$ =0.5 mA/V^2

The specifications are as follows:
1) Your design parameters are I_1, I_2 and R_D. You can select them as you wish.
2) The differential-mode gain ($A_{dm}=v_o/v_{id}$ when $v_1=+v_{id}/2$, $v_2=-v_{id}/2$) should be A_{dm}=10 V/V.
3) All transistors should operate in SAT.

Best design criteria is to have as low power dissipation (P) as possible.
Fill up the table with your design parameters.

Iter	Input Design Parameters			Output Parameters							
	I_1 (mA)	I_2 (mA)	R_D (kΩ)	V_{GS1} (V)	V_{DS1} (V)	V_{SG3} (V)	V_{SD3} (V)	V_{RD} (V)	A_{dm} (V/V)	A_{cm} (V/V)	P (mW)
1											
2											
3											
4											
5											